5V, 2A Synchronous Step-Down Regulator in 2mm × 2mm FCQFN

FEATURES

- **High Efficiency: 30mΩ NMOS, 85mΩ PMOS**
- **Peak Current Mode Control**
  - **27ns Minimum On-Time**
  - **Wide Bandwidth, Fast Transient Response**
- **Low-Ripple Burst Mode® Operation with I_Q of 80µA**
- **Up to 6MHz Operation**
- Safely Tolerates Inductor Saturation in Overload
- V_{IN} Range: 2.25V to 5.5V
- Fixed V_{OUT} Range: 0.5V to 3.65V, Factory Programmed in 50mV Steps
- V_{OUT} Accuracy: ±1% Overtemperature Range
- Precision 400mV Enable Threshold
- Shutdown Current: 1µA
- Power Good, Internal Compensation and Soft-Start
- Thermally Enhanced, 12-Pin, 2mm × 2mm, Flip Chip (FCQFN) Package with Side Wettable Flanks
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Optical Networking, Servers, Telecom
- Automotive, Industrial, Communications
- Distributed DC Power Systems (POL)
- FPGA, ASIC, µP Core Supplies

DESCRIPTION

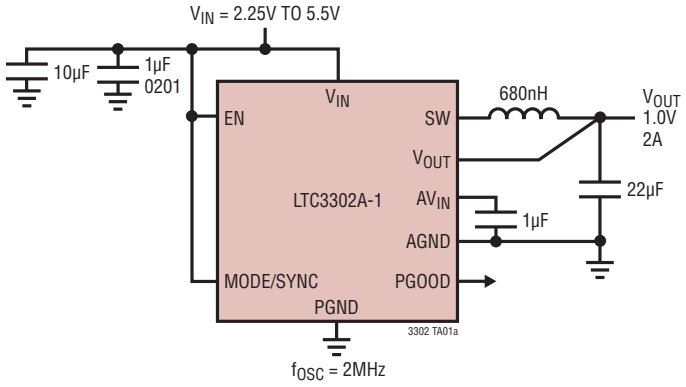
The LTC®3302 is a very small, high efficiency, low noise, monolithic synchronous 2A step-down DC/DC converter operating from a 2.25V to 5.5V input supply. Using constant frequency, peak current mode control, this regulator achieves fast transient response with small external components.

The LTC3302 operates in forced continuous or pulse-skipping mode for low noise, or in low-ripple Burst Mode operation for high efficiency at light loads, ideal for battery-powered systems. The IC regulates output voltages as low as 500mV. The adjustable version operates from 500mV to V_{IN} with two additional external resistors. Other features include output overvoltage protection, short-circuit protection, thermal shutdown, clock synchronization, and up to 100% duty cycle operation for low dropout.

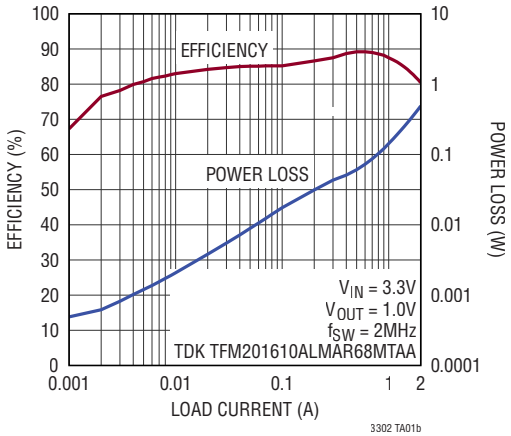
The LTC3302 is available in a low profile 2mm × 2mm FCQFN package with exposed pad and side wettable flanks.

TYPICAL APPLICATION

High Efficiency, 2MHz, 1V, 2A Step-Down Converter



Efficiency and Power Loss in Burst Mode Operation



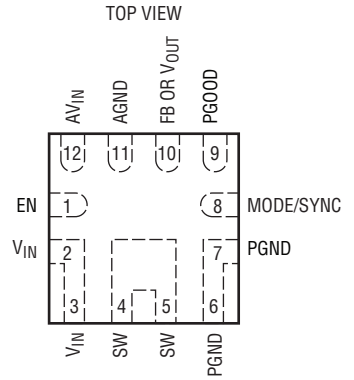
Rev. 0

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, AV_{IN} ..... –0.3V to 6V
EN ..... –0.3V to Lesser of (V_{IN} + 0.3V) or 6V
FB, V_{OUT} ..... –0.3V to Lesser of (V_{IN} + 0.3V) or 6V
MODE/SYNC ..... –0.3V to Lesser of (V_{IN} + 0.3V) or 6V
AGND to PGND ..... –0.3V to 0.3V
PGOOD ..... –0.3V to 6V
I_{PGOOD} 5mA
Operating Junction Temperature Range (Note 2):
LTC3302R ..... –40°C to +150°C
LTC3302J ..... –40°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
Maximum Reflow (Package Body) Temperature ... 260°C

PIN CONFIGURATION



FCQFN PACKAGE
12-PIN (2mm × 2mm × 0.75mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 48.9°C/W,
$\theta_{JCBOTTOM}$ = 6.4°C/W, θ_{JCTOP} = 85.6°C/W, Ψ_{JT} = 0.6°C/W
θ AND Ψ VALUES DETERMINED PER JESD51-7 ON A JEDEC 2S2P PCB

ORDER INFORMATION***

TAPE AND REEL	FREQUENCY****	PART MARKING*	PACKAGE TYPE	AMBIENT TEMPERATURE RANGE (T_A)
LTC3302ARUCM#TRPBF	2MHz	LHSK	FCQFN, 12-Pin, 2mm × 2mm × 0.75mm (Flip Chip Package with QFN Footprint)	–40°C to 125°C
LTC3302CRUCM#TRPBF	6MHz	LHSM	FCQFN, 12-Pin, 2mm × 2mm × 0.75mm (Flip Chip Package with QFN Footprint)	–40°C to 125°C
AUTOMOTIVE PRODUCTS**				
LTC3302AJUCM#WTRPBF	2MHz	LHSK	FCQFN, 12-Pin, 2mm × 2mm × 0.75mm (Flip Chip Package with QFN Footprint)	–40°C to 125°C
LTC3302AJUCM-1#WTRPBF	2MHz	LHTP	FCQFN, 12-Pin, 2mm × 2mm × 0.75mm (Flip Chip Package with QFN Footprint)	–40°C to 125°C
LTC3302AJUCM-1.2#WTRPBF	2MHz	LHTR	FCQFN, 12-Pin, 2mm × 2mm × 0.75mm (Flip Chip Package with QFN Footprint)	–40°C to 125°C
LTC3302AJUCM-1.8#WTRPBF	2MHz	LHTW	FCQFN, 12-Pin, 2mm × 2mm × 0.75mm (Flip Chip Package with QFN Footprint)	–40°C to 125°C
LTC3302CJUCM#WTRPBF	6MHz	LHSM	FCQFN, 12-Pin, 2mm × 2mm × 0.75mm (Flip Chip Package with QFN Footprint)	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500-unit reels through designated sales channels with #TRMPBF suffix.

Sample & Buy. Please see the website product page Sample and Buy Table for the list of available released options.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

***Fixed output versions are available from 0.5V to 3.65V in 50mV increments. Please contact marketing for availability.

****For 4MHz and 8MHz frequency versions, please contact Marketing for availability.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range (Note 2), otherwise specifications are at T_A = 25°C; V_{IN} = 4V, V_{EN} = V_{IN}, MODE/SYNC = Float, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply						
Operating Supply Voltage (V_{IN})		●	2.25		5.5	V
V_{IN} Undervoltage Lockout V_{IN} Undervoltage Lockout Hysteresis	V_{IN} Rising	●	2.0	2.1 150	2.2	V mV
V_{IN} Quiescent Current in Shutdown	V_{EN} = 0.1V			1	2	µA
V_{IN} Quiescent Current (Note 3)	Burst Mode Operation, Sleeping All Modes, Not Sleeping			80 1.2	120 2	µA mA
Enable Threshold Enable Threshold Hysteresis	V_{EN} Rising	●	0.375	0.4 50	0.425	V mV
EN Pin Leakage	V_{EN} = 0.5V		–20		20	nA
Voltage Regulation						
Regulated FB or Output Voltage (FB or V_{OUT})	% of Selected FB or V_{OUT}, 0.5V ≤ FB or V_{OUT} ≤ 3.65V	●	99	100	101	%
Feedback Voltage Line Regulation	V_{IN} = MAX (2.25V, V_{OUT} + 150mV) to 5.5V			0.015	0.05	%/V
Minimum On Time ($t_{ON,MIN}$)	V_{IN} = 5.5V	●		27	50	ns
Maximum Duty Cycle		●	100			%
Top Switch ON-Resistance				85		mΩ
Bottom Switch ON-Resistance				30		mΩ
Top Switch Current Limit ($I_{PEAKMAX}$)	V_{OUT}/V_{IN} ≤ 0.2		2.9	3.2	3.5	A
Bottom Switch Current Limit ($I_{VALLEYMAX}$)				2.7		A
Bottom Switch Reverse Current Limit (I_{REVMAX})	Forced Continuous Mode		–2.0	–1.0	–0.5	A
SW Leakage Current	V_{EN} = 0.1V		–100		100	nA
Power Good and Soft-Start						
PGOOD Rising Threshold PGOOD Hysteresis	As a Percentage of the Regulated V_{OUT}	● ●	97 0.7	98 1.2	99 1.7	% %
Overvoltage Rising Threshold Overvoltage Hysteresis	As a Percentage of the Regulated V_{OUT}	● ●	107 1	110 2.2	114 3.5	% %
PGOOD Delay				120		µs
PGOOD Pull-Down Resistance	V_{PGOOD} = 0.1V			10	20	Ω
PGOOD Leakage Current	V_{PGOOD} = 5.5V				20	nA
Soft-Start Duration		●	0.25	1	3	ms
Default Oscillator Frequency	LTC3302A	●	1.85	2	2.15	MHz
	LTC3302C	●	5.55	6	6.45	MHz
Oscillator and MODE/SYNC						
Frequency Synchronization Range	Percentage of Nominal Frequency Range	●	–20		20	%
Minimum SYNC High or Low Pulse Width		●	40			ns
SYNC Pulse Voltage Levels	Level High Level Low	● ●	1.2		 0.4	V V
MODE/SYNC No Clock Detect Time	Percentage of Nominal Period			50		%
MODE/SYNC Pin Threshold	For Programming Forced Continuous Mode For Programming Pulse-Skipping Mode For Programming Burst Mode Operation	● ● ●	 1.0 V_{IN} – 0.1	 Float	0.1 V_{IN} – 1.0	V V V

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3302 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3302R is guaranteed over the –40°C to 150°C operating junction temperature range. The LTC3302J is guaranteed over the –40° C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures above 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors. The junction temperature (T_J in °C) is calculated from ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

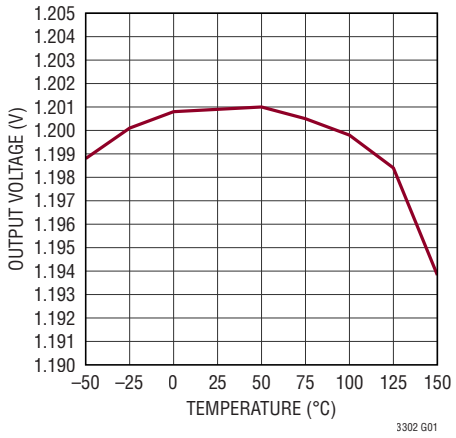
The LTC3302 includes overtemperature protection that protects the device during momentary overload conditions. Junction temperatures exceed 150°C when overtemperature protection is engaged. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: Supply current specification does not include switching currents. Actual supply currents are higher.

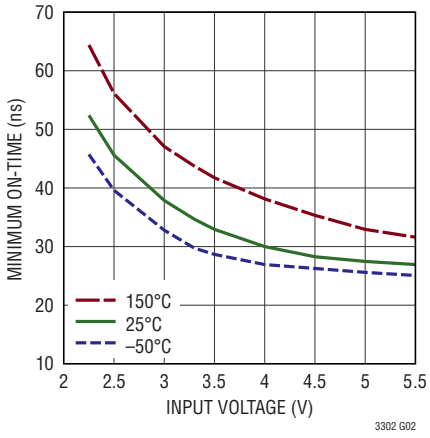
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, T_A = 25°C, unless otherwise noted.

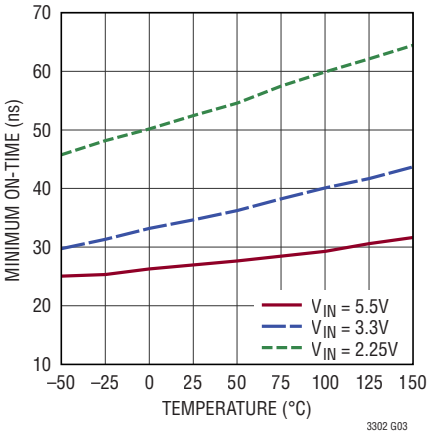
Normalized Regulation Voltage (to 1.2V) vs Temperature



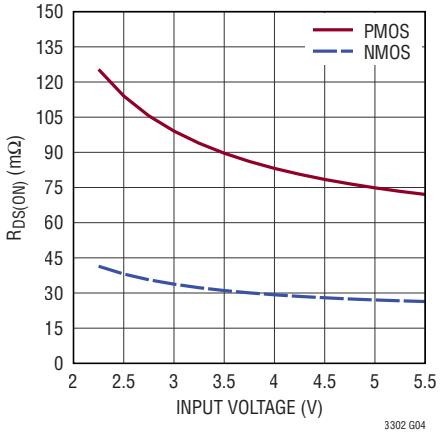
Minimum On-Time vs V_{IN}



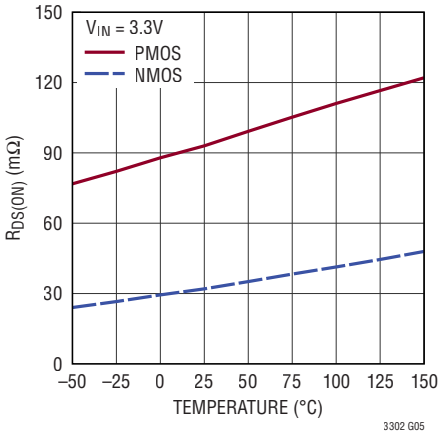
Minimum On-Time vs Temperature



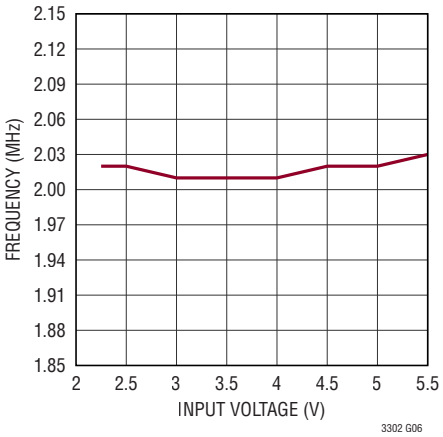
Switch On-Resistance vs V_{IN}



Switch On-Resistance vs Temperature



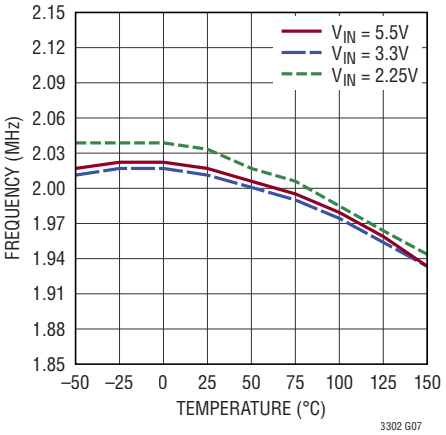
Switching Frequency vs V_{IN}



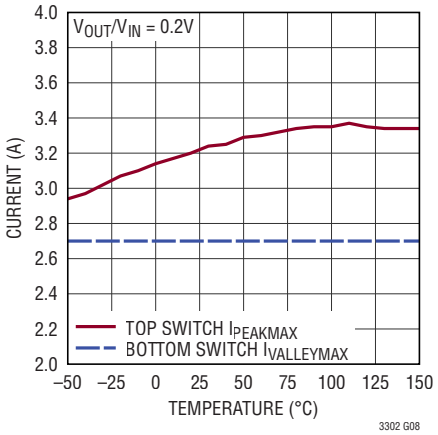
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, T_A = 25°C, unless otherwise noted.

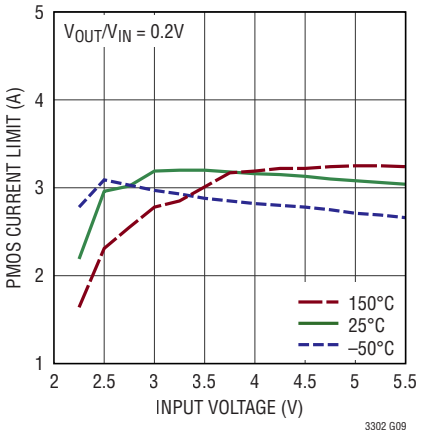
Switching Frequency vs Temperature



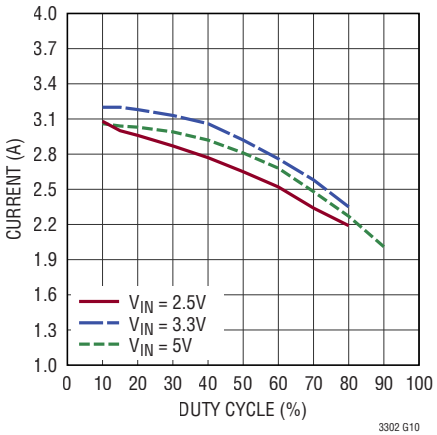
Switch Current Limits vs Temperature



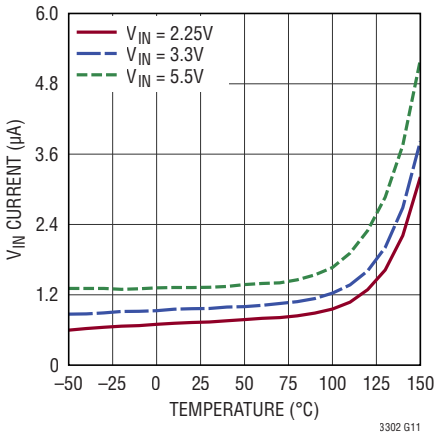
PMOS Current Limit vs V_{IN}



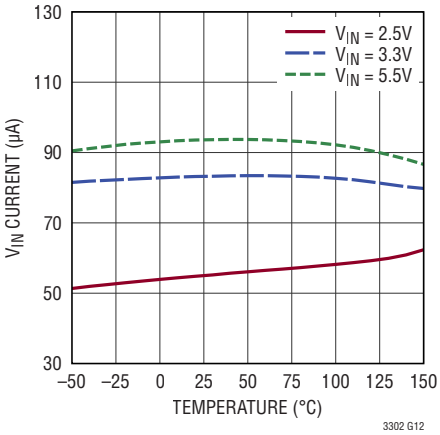
PMOS Current Limit vs Duty Cycle



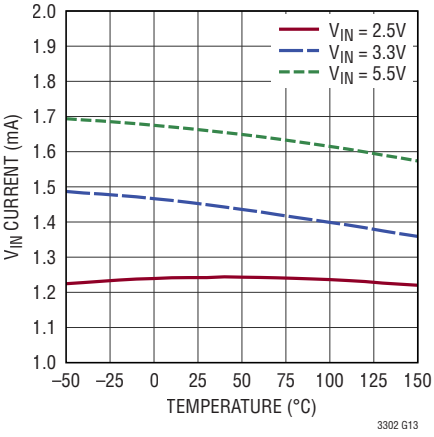
V_{IN} Shutdown Current vs Temperature



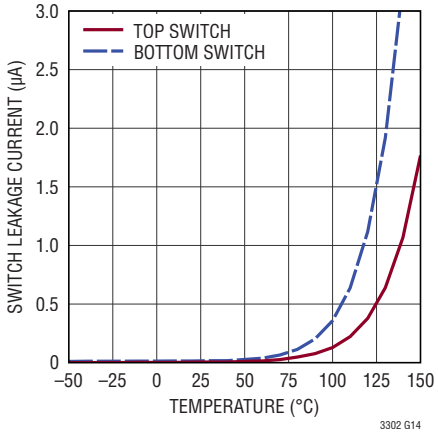
V_{IN} Quiescent Current, Burst Mode Operation, Sleeping



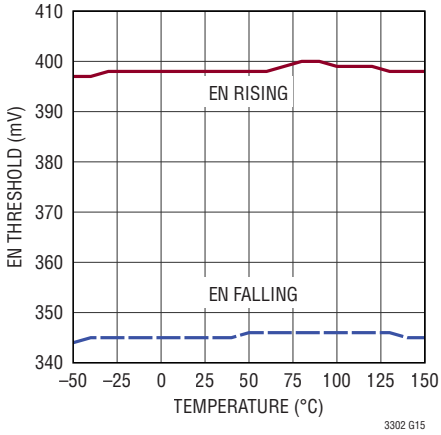
V_{IN} Quiescent Current All Modes, Not Sleeping



Switch Leakage vs Temperature

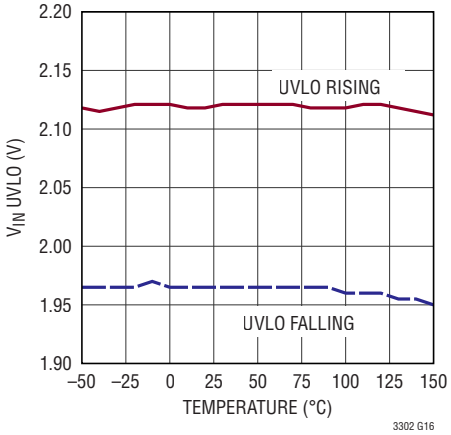


EN Threshold vs Temperature

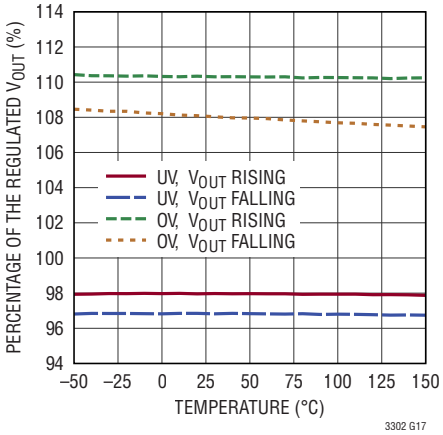


TYPICAL PERFORMANCE CHARACTERISTICS V_{IN} = 3.3V, T_A = 25°C, unless otherwise noted.

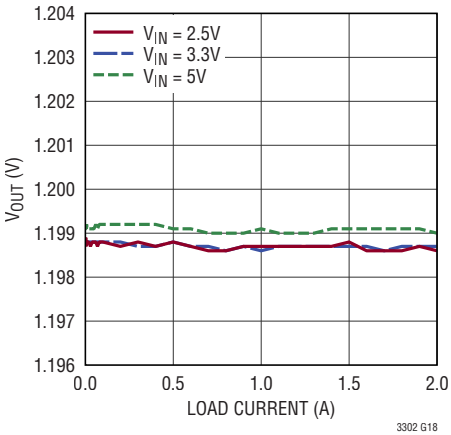
V_{IN} UVLO Threshold vs Temperature



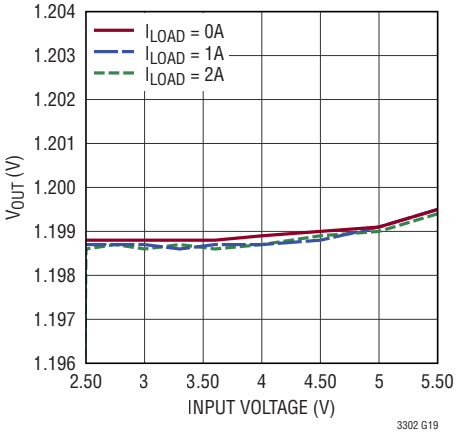
UV, OV PGOOD Thresholds vs Temperature



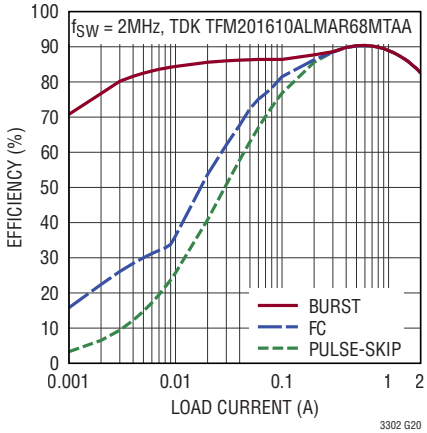
V_{OUT} Load Regulation, V_{OUT} = 1.2V Application, Forced Continuous Mode



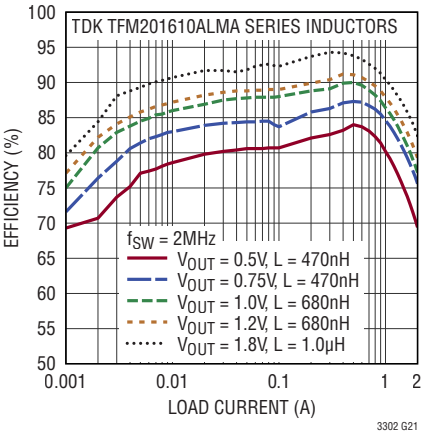
V_{OUT} Line Regulation, V_{OUT} = 1.2V Application, Forced Continuous Mode



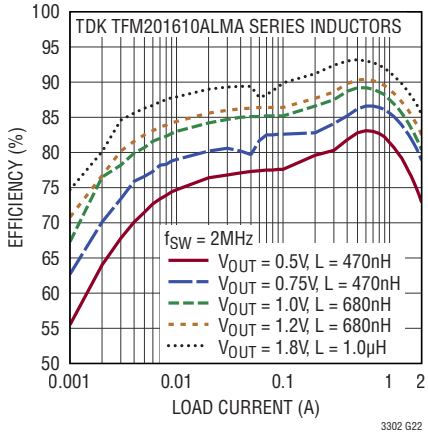
Efficiency vs Load, All Modes, V_{IN} = 3.3V, V_{OUT} = 1.2V



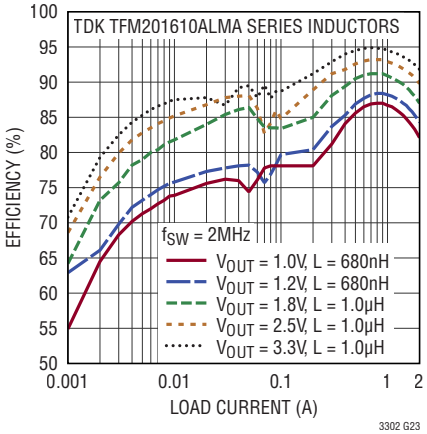
Efficiency, V_{IN} = 2.5V, Burst Mode Operation



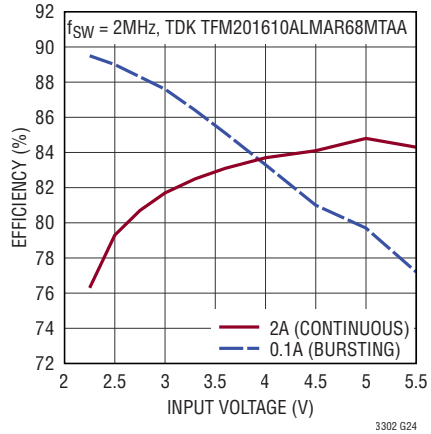
Efficiency, V_{IN} = 3.3V, Burst Mode Operation



Efficiency, V_{IN} = 5.0V, Burst Mode Operation



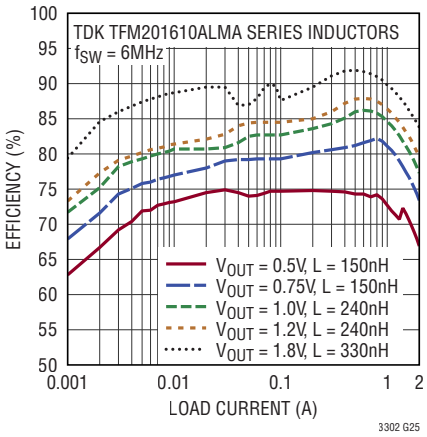
Efficiency vs V_{IN}, V_{OUT} = 1.2V



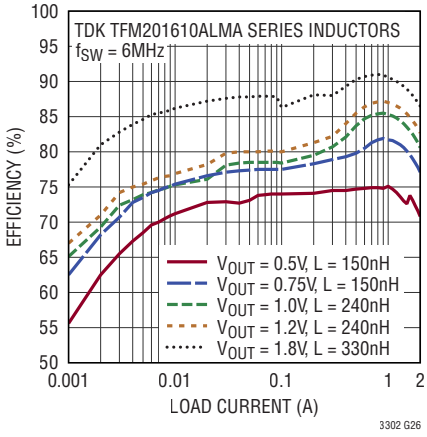
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, T_A = 25°C, unless otherwise noted.

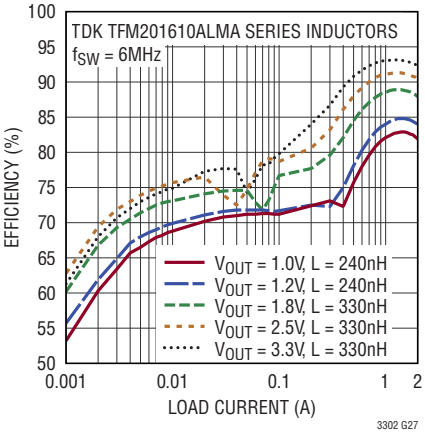
Efficiency, V_{IN} = 2.5V, Burst Mode Operation



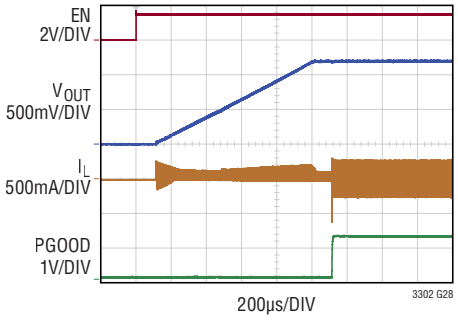
Efficiency, V_{IN} = 3.3V, Burst Mode Operation



Efficiency, V_{IN} = 5V, Burst Mode Operation

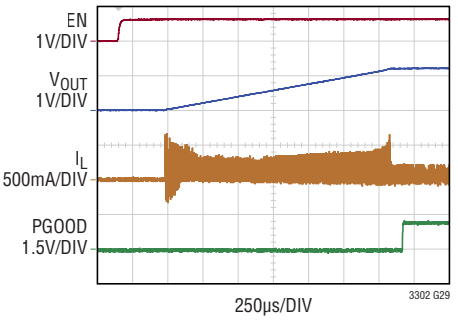


Start-Up Waveforms, Forced Continuous Mode



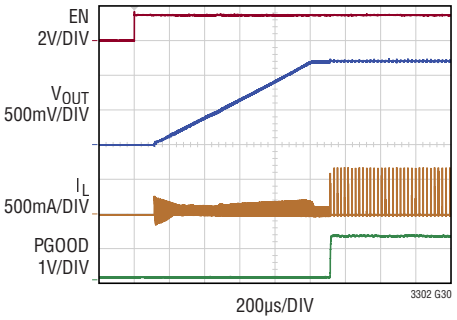
3.3V TO 1.2V, 2MHz
R_{LOAD} = 120Ω

Start-Up Waveforms, Pulse-Skipping Mode



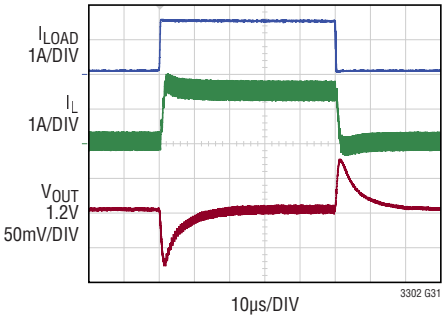
3.3V TO 1.2V, 2MHz
R_{LOAD} = 120Ω

Start-Up Waveforms, Burst Mode Operation



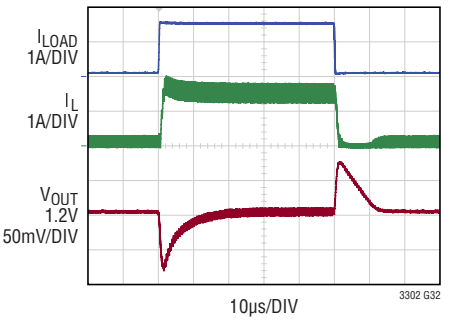
3.3V TO 1.2V, 2MHz
R_{LOAD} = 120Ω

Load Transient Response, Forced Continuous Mode



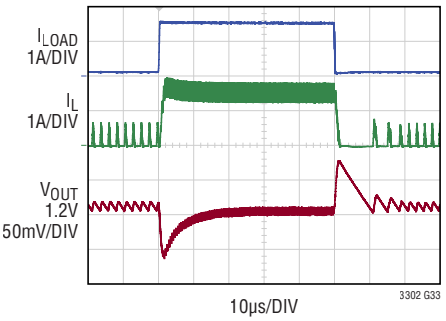
3.3V TO 1.2V, 2MHz
C_{OUT} = 20µF, L = 680nH
LOAD STEP: 0.1A TO 1.5A AT 5A/µs

Load Transient Response, Pulse-Skipping Mode



3.3V TO 1.2V, 2MHz
C_{OUT} = 20µF, L = 680nH
LOAD STEP: 0.1A TO 1.5A AT 5A/µs

Load Transient Response, Burst Mode Operation



3.3V TO 1.2V, 2MHz
C_{OUT} = 20µF, L = 680nH
LOAD STEP: 0.1A TO 1.5A AT 5A/µs

PIN FUNCTIONS

EN (Pin 1): The EN pin has a precision enable threshold with hysteresis. An external resistor divider, from V_{IN} or from another supply, can be used to program the threshold below which the LTC3302 shuts down. If the precision threshold is not required, tie EN directly to V_{IN}. When the EN pin is low the LTC3302 enters a low current shutdown mode where all internal circuitry is disabled. Do not float this pin.

V_{IN} (Pins 2, 3): The V_{IN} pins supply current to the topside power switch. Connect both V_{IN} pins together with a short, wide trace and bypass to PGND with a low-ESR capacitor located as close to the pins as possible.

SW (Pins 4, 5): The SW pins are the switching outputs of the internal power switches. Connect these pins together and to the inductor with a short, wide trace.

PGND (Pins 6, 7): The PGND pins are the return path of the internal bottom side power switch. Connect the negative terminals of the input capacitors as close to the PGND pins as possible.

MODE/SYNC (Pin 8): The MODE/SYNC pin is a mode selection and external clock synchronization input. Float this pin to enable pulse-skipping mode at light loads. For higher efficiency at light loads, tie this pin to AV_{IN} to enable low-ripple Burst Mode operation. For faster transient response, lower noise, and full frequency operation over a wide load range, connect this pin to AGND to enable forced continuous mode. Drive MODE/SYNC with an external clock to synchronize the switcher to the applied frequency. While synchronizing, the part operates in forced continuous mode.

PGOOD (Pin 9): The PGOOD pin is the open-drain output of an internal power good comparator. When the regulated output voltage falls below the PGOOD threshold or rises above the overvoltage threshold, this pin is pulled low. When V_{IN} is above the UVLO threshold and the part is in shutdown, this pin is also pulled low.

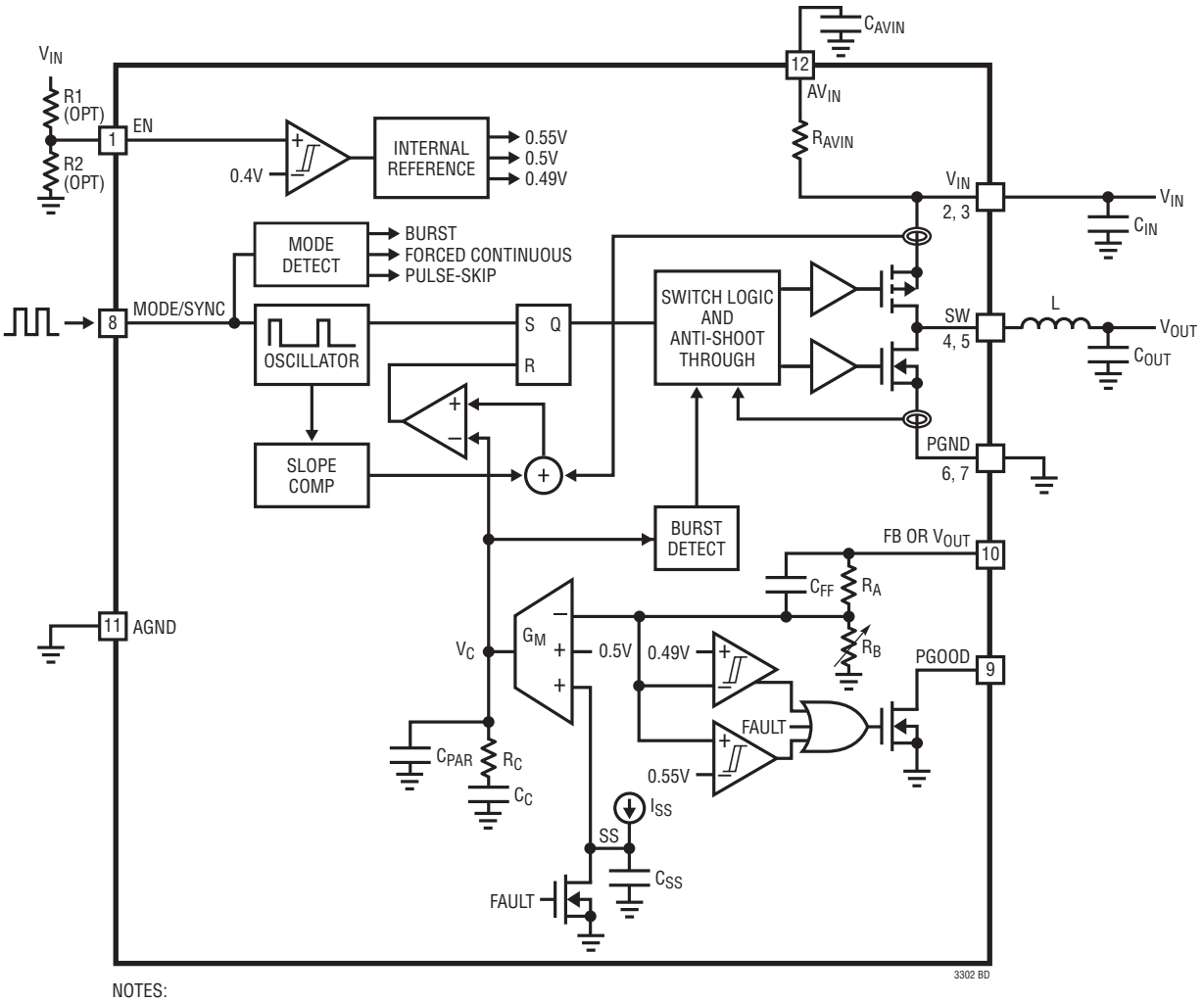
FB (Pin 10): FB is the output voltage feedback pin for the LTC3302 adjustable version. The FB pin is regulated to 500mV. Program the output voltage and close the control loop by connecting this pin to the middle node of a resistor divider between the regulator output and AGND.

V_{OUT} (Pin 10): V_{OUT} is the regulated output voltage pin for the LTC3302 fixed voltage versions. For the fixed V_{OUT} versions, connect this pin directly to the regulator output. Connect a low-ESR capacitor from this node to AGND.

AGND (Pin 11): The AGND pin is the output voltage remote ground sense. Connect the AGND pin directly to the negative terminal of the output capacitor at the load. The AGND pin is also the ground reference for the internal analog circuitry. Place a 1µF ceramic bypass capacitor as close as possible to the AV_{IN} and AGND pins. Connect FB return to AGND as well.

AV_{IN} (Pin 12): The AV_{IN} pin supplies current to the internal analog circuitry. Decouple this pin to AGND with a 1µF low-ESR capacitor to AGND.

BLOCK DIAGRAM



NOTES:

FOR THE LTC3302 ADJUSTABLE VERSION, PIN 10 IS FB. FB IS HIGH IMPEDANCE AND RB RESISTANCE IS INFINITE. THE FB PIN REGULATES TO THE 500mV TARGET.

FOR THE LTC3302 FIXED OUTPUT VOLTAGE VERSIONS, PIN 10 IS V_{OUT}. RB IS INTERNALLY SET FOR THE REGULATION TARGET. THE V_{OUT} PIN IS NOT HIGH IMPEDANCE AND REGULATES TO THE OUTPUT VOLTAGE TARGET.

OPERATION

Voltage Regulation

The LTC3302 is a 5V, 2A monolithic, constant frequency, peak current mode control, step-down DC/DC converter. The synchronous buck switching regulators are internally compensated and require only external feedback resistors to set the output voltage. An internal oscillator, with the frequency factory programmed or synchronized to an external clock, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor ramps up until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by an internal V_C voltage. The error amplifier regulates V_C by comparing the voltage on the FB node with an internal 500mV reference. An increase in the load current causes a reduction in the feedback voltage relative to the reference, causing the error amplifier to raise the V_C voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on and ramps down the inductor current for the remainder of the clock cycle or, if in pulse-skipping or Burst Mode operation, until the inductor current falls to zero. If an overload condition results in excessive current flowing through the bottom switch, the next clock cycle is skipped until switch current returns to a safe level.

The enable pin has a precision 400mV threshold to provide event-based power-up sequencing by connecting the EN pin to the output of another buck through a resistor divider. If the EN pin is low, the device is shut down and in a low quiescent current state. When the EN pin is above its threshold, the switching regulator enables.

The LTC3302 has forward and reverse inductor current limiting, short-circuit protection, output overvoltage protection, and soft-start to limit inrush current during start-up or recovery from a short-circuit.

Mode Selection

The LTC3302 operates in three modes set by the MODE/SYNC pin: pulse-skipping (when the MODE/SYNC pin is floating), forced continuous (when the MODE/SYNC pin is set low), and Burst Mode operation (when the MODE/SYNC pin is set high).

In pulse-skipping mode, the oscillator operates continuously and positive SW transitions are aligned to the clock. Negative inductor current is disallowed and, during light loads, switch pulses are skipped to regulate the output voltage.

In forced continuous mode, the oscillator operates continuously. The top switch turns on every cycle and regulation is maintained by allowing the inductor current to reverse at light load. This mode allows the buck to run at a fixed frequency with minimal output ripple. In forced continuous mode, if the inductor current reaches I_{REVMAX} (into the SW pin), the bottom switch turns off for the remainder of the cycle to limit the current.

In Burst Mode operation at light loads, the output capacitor is charged to a voltage slightly higher than its regulation point. The regulator then goes into a sleep state, during which time the output capacitor provides the load current. In sleep, most of the regulator's circuitry is powered down, helping conserve input power. When the output voltage drops below its programmed value, the circuitry is powered on and another burst cycle begins. The sleep time decreases as load current increases. In Burst Mode operation, the regulator bursts at light loads, whereas at higher loads it operates in constant frequency PWM mode.

OPERATION

Synchronizing the Oscillator to an External Clock

The LTC3302's internal oscillator can be synchronized to an external frequency by applying a square wave clock signal to the MODE/SYNC pin. During synchronization, the top power switch turn-on is locked to the rising edge of the external frequency source. While synchronizing, the switcher operates in forced continuous mode. The synchronization frequency range is ±20% of the nominal frequency.

After detecting an external clock on the MODE/SYNC pin, the rising edge of the internal clock is compared with the rising edge of the external clock. When the edges are aligned, the LTC3302 switches over to the external clock. If the external clock is removed for more than 1.5 clock cycles, the clock instantly reverts back to the internal clock.

Output Power Good

When the LTC3302's output voltage is within the –2%/+10% window of the nominal regulation voltage the output is considered good and the open-drain PGOOD pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device pulls the PGOOD pin low. The PGOOD pin is also pulled low during the following fault conditions: EN pin is low, V_{IN} is too low, or thermal shutdown. To filter noise and short duration output voltage transients, the lower threshold has a hysteresis of 1.2%, the upper threshold has a hysteresis of 2%, and both have a built-in time delay to report PGOOD, typically 120µs.

Output Overvoltage Protection

During an output overvoltage event, when the FB pin voltage is greater than 110% of nominal, the LTC3302 top power switch turns off. If the output remains out of regulation for more than 120µs, the PGOOD pin is pulled low.

An output overvoltage event should not happen under normal operating conditions.

Overtemperature Protection

To prevent thermal damage to the LTC3302 and its surrounding components, the device incorporates an overtemperature (OT) function. When the die temperature reaches 165°C (typical, not tested) the switcher is shut down and remains in shutdown until the die temperature falls to 160°C (typical, not tested).

Output Voltage Soft-Start

Soft-starting the output prevents current surge on the input supply and/or output voltage overshoot. During soft-start, the output voltage proportionally tracks the internal node voltage ramp. An active pull-down circuit discharges that internal node in the case of fault conditions. The ramp restarts when the fault is cleared. Fault conditions that initiate the soft-start ramp are the EN pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Dropout Operation

As the input supply voltage approaches the output voltage, the duty cycle increases toward 100%. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle, eventually reaching 100% duty cycle. The output voltage is then determined by the input voltage minus the DC voltage drop across the internal P-channel MOSFET and the inductor.

Low Supply Operation

The LTC3302 is designed to operate down to an input supply voltage of 2.25V. One important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the internal power switches increases. Calculate the worst case LTC3302 power dissipation and die junction temperature at the lowest input voltages.

OPERATION

Output Short-Circuit Protection and Recovery

The peak inductor current level, at which the current comparator shuts off the top power switch, is controlled by the internal V_C voltage. When the output current increases, the error amplifier raises V_C until the average inductor current matches the load current. The LTC3302 clamps the maximum V_C voltage, thereby limiting the peak inductor current.

When the output is shorted to ground, the inductor current decays very slowly when the bottom power switch is on because the voltage across the inductor is small. To keep the inductor current under control, a secondary limit is imposed on the valley of the inductor current. If the inductor current measured through the bottom power switch remains greater than $I_{VALLEYMAX}$ at the end of the cycle, the top power switch is held off. Subsequent switching cycles are skipped until the inductor current falls below $I_{VALLEYMAX}$.

Recovery from an output short-circuit may involve a soft-start cycle if V_{FB} falls more than approximately 100mV below regulation. During such a recovery, V_{FB} quickly charges up by that ~100mV and then follow the soft-start ramp until regulation is reached.

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Refer to the Block Diagram for reference.

FB Resistor Network (LTC3302 Adjustable Version)

The output voltage for the LTC3302 adjustable version is programmed by a resistor divider between the output and the FB pin. Choose the resistor values according to Equation 1.

$$R_A = R_B\left(\frac{V_{OUT}}{500mV} - 1\right) \quad (1)$$

as shown in Figure 1:

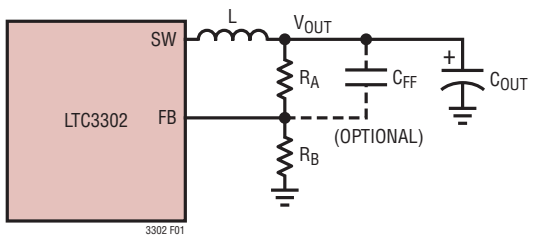

Figure 1. Feedback Resistor Network for the LTC3302 Adjustable Version

The adjustable version can have an output voltage from 0.5V to V_{IN}.

Reference designators refer to the Block Diagram. Typical values for R_B range from 10k to 400k. 0.1% resistors are recommended to maintain output voltage accuracy. The buck regulator transient response may improve with an optional phase lead capacitor C_{FF} that helps cancel the pole created by the feedback resistors and the input capacitance of the FB pin. Experimentation with capacitor values between 2pF and 50pF may improve transient response. The values used in the typical application circuits are a good starting point.

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, transient response, and input voltage range.

The advantage of high frequency operation is that smaller inductor and capacitor values may be used. Higher switching frequencies allow for higher control loop bandwidth and, therefore, faster transient response. The disadvantages of higher switching frequencies are lower efficiency, because of increased switching losses, and a smaller input voltage range, because of minimum switch on-time limitations.

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The minimum on-time of the buck regulator imposes a minimum operating duty cycle. The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated with Equation 2.

$$f_{SW(MAX)} = \frac{V_{OUT}}{t_{ON(MIN)} \bullet V_{IN(MAX)}} \quad (2)$$

where $V_{IN(MAX)}$ is the maximum input voltage, V_{OUT} is the output voltage, and $t_{ON(MIN)}$ is the minimum top switch on-time. This equation shows that a slower switching frequency is necessary to accommodate a high $V_{IN(MAX)}/V_{OUT}$ ratio.

The LTC3302 is capable of a maximum duty cycle of 100%, therefore, the V_{IN}-to-V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch, the inductor DCR, and the load current.

Setting the Switching Frequency

The LTC3302 uses a constant frequency peak current mode control architecture. The switching frequency is factory programmed to one of four values: 2MHz, 4MHz, 6MHz, or 8MHz. Higher frequencies increase switching losses and reduce efficiency, but could potentially allow for smaller external components.

The LTC3302's internal oscillator can be synchronized to an external frequency by applying a square wave clock signal to the MODE/SYNC pin. The synchronization frequency range is ±20% of the nominal, factory programmed frequency.

When the rising edge at the MODE/SYNC pin is aligned to the internal clock, the LTC3302 switches over to the external clock. If the external clock is removed for more than 1.5 clock cycles, the clock instantly reverts back to the internal clock.

Inductor Selection and Maximum Output Current

Considerations in choosing an inductor are inductance, RMS current rating, saturation current rating, DCR, and core loss.

Select the inductor value based on Equation 3 and Equation 4.

$$L \approx \frac{V_{OUT}}{0.6A \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} \leq 0.5 \quad (3)$$

$$L \approx \frac{0.25 \bullet V_{IN(MAX)}}{0.6A \bullet f_{SW}} \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} > 0.5 \quad (4)$$

where f_{SW} is the switching frequency, V_{OUT} is the output voltage, and $V_{IN(MAX)}$ is the maximum input voltage.

To avoid overheating of the inductor choose an inductor with an RMS current rating that is greater than the maximum expected output load of the application. Overload and short-circuit conditions need to be taken into consideration.

In addition, ensure that the saturation current rating (typically labeled I_{SAT}) of the inductor is higher than the maximum expected load current plus half the inductor ripple current given by Equation 5.

$$I_{SAT} > I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L \quad (5)$$

where $I_{LOAD(MAX)}$ is the maximum output load current for a given application and ΔI_L is the inductor ripple current calculated with Equation 6.

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

A more conservative choice would be to use an inductor with an I_{SAT} rating higher than the maximum current limit of the LTC3302.

To keep the efficiency high, choose an inductor with the lowest series resistance (DCR). The core material should be intended for high frequency applications. Table 1 shows recommended inductors from several manufacturers.

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Table 1. Recommended Inductors with Typical Specifications

MANUFACTURER	INDUCTOR FAMILY	INDUCTANCE (nH)	I_{TEMP} (A)*	I_{SAT} (A)	DCR (mΩ)	W × L × H (mm)
Murata	DFE18SAN-E0	240	3.2	4.2	36	1.6 × 0.8 × 0.8
Murata	DFE18SAN-G0	240	3.5	4.9	30	1.6 × 0.8 × 1.0
Murata	DFE201210S	110, 470	6.3, 4.0	11, 5.3	8, 27	2.0 × 1.2 × 1.0
Murata	DFE201210U	240 to 470	3.8 to 3.0	6.5 to 4.4	20 to 34	2.0 × 1.2 × 1.0
Murata	DFE201610E	240 to 680	5.5 to 3.7	7.0 to 4.8	16 to 36	2.0 × 1.6 × 1.0
Murata	DFE201612E	240 to 680	6.0 to 4.1	7.8 to 4.8	13 to 27	2.0 × 1.6 × 1.2
Murata	DFE201612PD	150	5.2	6.2	12	2.0 × 1.6 × 1.2
Murata	DFE252010F	330 to 680	5.6 to 4.1	7.6 to 5.5	16 to 31	2.5 × 2.0 × 1.0
Murata	DFE252012F	330 to 680	6.0 to 4.6	8.5 to 6.0	14 to 25	2.5 × 2.0 × 1.2
Vishay	IHHP-0806AB-01	220 to 470	5.3 to 4.2	5.8 to 4.4	13 to 29	2.0 × 1.6 × 1.2
Vishay	IHHP-1008AB-01	220 to 680	7.4 to 3.8	7.1 to 4.1	8.4 to 28	2.5 × 2.0 × 1.2
XFRMS	XFHCL43LT	220 to 470	8.0 to 4.5	7.0 to 3.8	13 to 25 (Max)	2.5 × 2.0 × 1.2
NIC	NPMH0805B	240, 470	4.2, 3.0	4.8, 3.2	25, 48 (Max)	2.0 × 1.2 × 0.8
NIC	NPMH0805C	240 to 470	3.7 to 3.0	4.5 to 3.3	28 to 42 (Max)	2.0 × 1.2 × 1.0
NIC	NPMH0806C	240 to 470	4.7 to 3.5	5.6 to 3.9	23 to 42 (Max)	2.0 × 1.6 × 1.0
NIC	NPIM26LP	240 to 680	6.5 to 4.2	7.5 to 5.1	15 to 36	2.0 × 1.6 × 1.0
NIC	NPIM20LP	240 to 680	6.0 to 4.4	9.5 to 5.5	18 to 32	2.5 × 2.0 × 1.0
Sumida	201610CDMCC/DS	240, 470	5.2, 3.8	6.5, 4.2	19, 34	2.2 × 1.8 × 1.0
Sumida	252010CDMCC/DS	330 to 1000	5.2 to 3.2	6.8 to 3.8	16 to 46	2.7 × 2.2 × 1.0
Wurth Electronik	WE-PMMI-0805LP	110	3	6	24	2.0 × 1.2 × 0.6
Wurth Electronik	WE-PMMI-0806	240 to 470	3.5 to 3.0	4.0 to 3.4	15 to 20	2.0 × 1.6 × 0.6
Wurth Electronik	WE-PMCI-0806	240, 470	3.6, 2.9	5.4, 4.2	19, 34	2.0 × 1.6 × 1.0
Wurth Electronik	WE-PMCI-1008	470	3.3	5	25	2.5 × 2.0 × 1.0
Wurth Electronik	WE-LQS-2512	160	3.7	6.4	16	2.5 × 2.0 × 1.2
TDK	TFM201208BLD	110	6.8	8.8	10	2.0 × 1.2 × 0.8

*Strongly depends on the PCB thermal properties

Input Capacitors

Bypass the input of the LTC3302 with a ceramic capacitor from V_{IN} to PGND, close to the part. This capacitor should be 0603 or 0805 in size. A smaller, optional 0201 capacitor can also be placed as close as possible to the LTC3302 directly on the traces leading from V_{IN} (Pin 3) and PGND (Pin 6) for better performance with minimal (if at all) increase in application footprint. See PCB Layout Considerations section for more detail. X7R or X5R capacitors are recommended for best performance across temperature and input voltage variations (see Table 2).

Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with an electrolytic capacitor.

A ceramic input capacitor combined with trace or cable inductance forms a high quality (underdamped) tank circuit. If the LTC3302 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LTC3302's voltage rating. This situation is easily avoided (see Application Note AN88).

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Table 2. Ceramic Capacitor Manufacturers

VENDOR	URL
AVX	www.avxcorp.com
Murata	www.murata.com
TDK	www.tdk.com
Taiyo Yuden	www.t-yuden.com
Samsung	www.samsungsem.com
Wurth Elektronik	www.we-online.com

Output Capacitor, Output Ripple, and Transient Response

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LTC3302 at the SW pin to produce the DC output. In this role, it determines the output ripple; thus, low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LTC3302's control loop. The LTC3302 is internally compensated and has been designed to operate at a high bandwidth for fast transient response capability. The selection of C_{OUT} affects the bandwidth of the system, but the transient response is also affected by V_{OUT}, V_{IN}, f_{SW}, and other factors. A good place to start is with the output capacitance value given by Equation 7.

$$C_{OUT} = 20 \bullet \frac{I_{MAX}}{f_{SW}} \sqrt{\frac{0.5}{V_{OUT}}} \quad (7)$$

where C_{OUT} is the recommended output capacitor value in µF, f_{SW} is the switching frequency in MHz, I_{MAX} = 2A is the rated output current in Amps, and V_{OUT} is in Volts.

A lower value output capacitor saves space and cost but transient performance suffers and loop stability must be verified.

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best output ripple and transient performance. Use X5R or X7R ceramic capacitors (see Table 2). Even better output ripple and transient performance can be achieved by using low-ESL reverse geometry or three-terminal ceramic capacitors.

During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop increases the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation components and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. Although affected by V_{OUT}, V_{IN}, f_{SW}, $t_{ON(MIN)}$, the equivalent series inductance (ESL) of the output capacitor, and other factors, the output droop, V_{DROOP}, is usually about 3 times the linear drop of the first cycle given by Equation 8.

$$V_{DROOP} = \frac{3 \bullet \Delta I_{OUT}}{C_{OUT} \bullet f_{SW}} \quad (8)$$

where ΔI_{OUT} is the load step.

Transient performance and control loop stability can be improved with a higher C_{OUT} and/or the addition of a feedforward capacitor C_{FF} placed between V_{OUT} and FB. Capacitor C_{FF} provides phase lead compensation by creating a high frequency zero which improves the phase margin and the high-frequency response. The values used in the typical application circuits are a good starting point. LTpowerCAD® is a useful tool to help optimize C_{FF} and C_{OUT} for a desired transient performance.

Applying a load transient and monitoring the response of the system or using a network analyzer to measure the actual loop response are two ways to experimentally verify transient performance and control loop stability, and to optimize C_{FF} and C_{OUT}.

When using the load transient response method to stabilize the control loop, apply an output current pulse of 20% to 100% of full load current having a very fast rise time. This produces a transient on the output voltage. Monitor V_{OUT} for overshoot or ringing that might indicate a stability problem (see Application Note AN149).

Output Voltage Sensing

The LTC3302's AGND pin is the ground reference for the internal analog circuitry, including the bandgap voltage reference. To achieve good load regulation connect the AGND pin to the negative terminal of the output capacitor

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(C_{OUT}) at the load. Any drop in the high current power ground return path is compensated. The AGND node carries very little current and, therefore, can be a minimal size trace. Place a small analog bypass 0201 or 0402 ceramic capacitor as close as possible to the LTC3302 directly on the traces leading from AV_{IN} (Pin 12) and AGND (Pin 11). All of the signal components, such as the FB resistor dividers, should be referenced to the AGND node. See the recommended PCB Layout (Figure 3) for more information.

Enable Threshold Programming

The LTC3302 has a precision threshold enable pin to enable or disable the switching. When forced low, the device enters a low current shutdown mode.

The rising threshold of the EN comparator is 400mV, with 50mV of hysteresis. The EN pin can be tied to V_{IN} if the shutdown feature is not used. Adding a resistor divider from V_{IN} to EN programs the LTC3302 to regulate the output only when V_{IN} is above a desired voltage (see Figure 2). Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws near constant power from its input source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where problems may occur. This threshold can be adjusted by setting the values R1 and R2 such that they satisfy Equation 9.

$$V_{IN(EN)} = \left(\frac{R1}{R2} + 1\right) \bullet 400mV \qquad (9)$$

as shown in Figure 2:

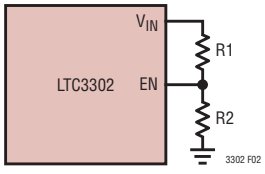

Figure 2. EN Divider

The LTC3302 remains off until V_{IN} is above $V_{IN(EN)}$. The buck regulator remains enabled until V_{IN} falls to $0.875 \bullet V_{IN(EN)}$ and EN is 350mV.

Alternatively, a resistor divider from an output of an upstream regulator to the EN pin of the LTC3302 provides event-based power-up sequencing, enabling the LTC3302 when the output of the upstream regulator reaches a predetermined level (e.g. 90% of the regulated output). Replace $V_{IN(EN)}$ in Equation 9 with that predetermined level.

PCB Layout Considerations

The LTC3302 is a high performance IC designed for high efficiency and fast transient response. For optimal results carefully consider the layout of the PCB board and follow the recommendations below to ensure proper operation. See Figure 3 for a recommended PCB layout.

1. The V_{IN} input supply pins (Pins 2, 3) should have local de-coupling capacitors to the PGND pins (Pins 6, 7). These capacitors provide the AC current to the internal power MOSFETs and their drivers. Large, switched currents flow in these capacitors and it is important to minimize inductance from these capacitors and their PCB traces to the V_{IN} and PGND pins.
   - Choose a small case size, such as 0603, and place close to the pins on the top side of the board.
   - To further reduce de-coupling inductance, a smaller 0201 capacitor can be placed in parallel, as close as possible to the V_{IN} and PGND pins.
   - See C_{IN1} and C_{IN2} placement in Figure 3, the recommended PCB layout.
2. Place the regulator inductor on the same side of the board as the LTC3302, minimizing parasitic inductance from the V_{OUT} side of the inductor and the C_{OUT} capacitors. The power trace connecting SW to the inductor should be wide and on PCB metal layer 2, with as many vias as allowed to minimize added parasitic inductance.
3. Solder the PGND pins (Pins 6, 7) directly to a ground plane on the top layer. Connect the top layer ground plane to ground plane(s) on lower levels with many

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thermal vias. These layers spread heat dissipated by the LTC3302.

4. Connect the ground side of any FB and EN components to AGND (Pin 11). Connect a 1µF de-coupling capacitor from AV_{IN} (Pin 12) to AGND. Power the AV_{IN} pin by connecting a 10Ω filter resistor from the V_{IN} supply to AV_{IN}.

   Connect the AGND pin to the rest of the PCB ground plane in only one location, to prevent transient currents in the ground plane from also flowing through the AGND trace. Optionally, connect the AGND pin to the negative terminal of the output capacitor at the load. This reduces any load regulation caused by voltage drops between the ground at the load and the LTC3302 voltage reference ground. The AGND node carries very little current and can be a minimal size trace.

5. Care should be taken in the layout of the PCB to ensure good heat sinking of the LTC3302. The heat generated internal to the package is concentrated near the power MOSFETs and mostly flows out of the V_{IN} and PGND pins to be spread on the PCB.

Connect the PGND pins (Pins 6, 7) to a large metal area on the top layer. Connect the top layer ground metal to ground plane(s) on lower levels with many thermal vias. These layers spread heat dissipated by the LTC3302. Also, connect the V_{IN} pins (Pins 2, 3) to a large metal plane with low thermal impedance.

The junction temperature, T_J, is calculated from the ambient temperature, T_A as given by Equation 10.

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (10)$$

Where θ_{JA} is approximately 37.6°C/W to 48.9°C/W, layout dependent.

Power dissipation within the LTC3302 is estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss.

The LTC3302 evaluation kit PCB has a θ_{JA} that is approximately 37.6°C/W, compared to approximately 48.9°C/W for a JEDEC 2S2P PCB. This is a 25% reduction in thermal impedance, and an example for how much a good layout can improve thermal performance.

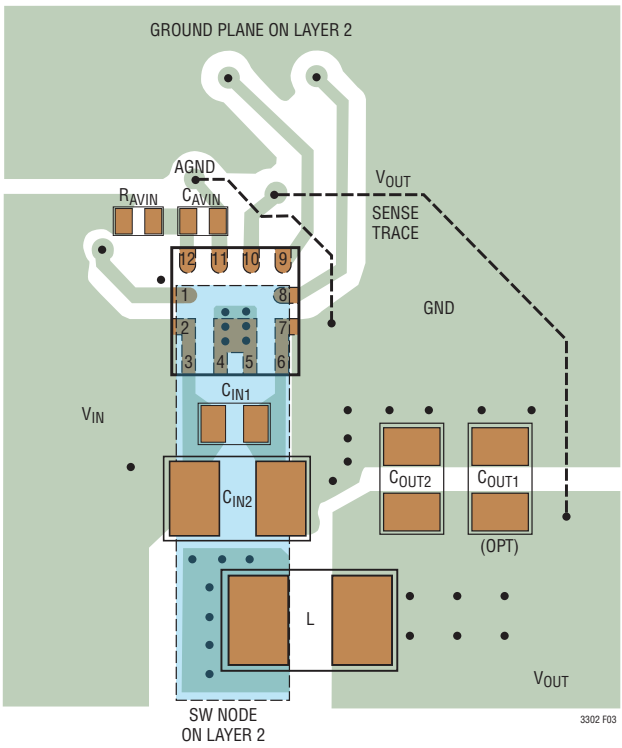
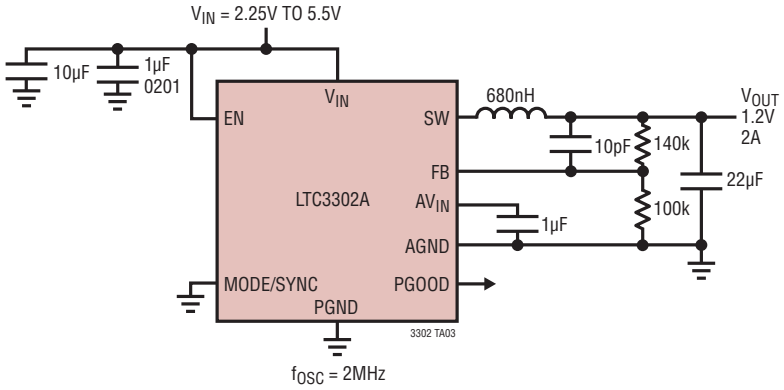


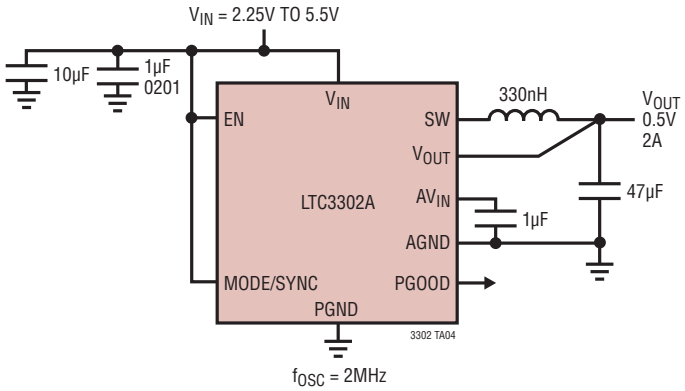
Figure 3. Recommended PCB Layout

TYPICAL APPLICATIONS

2MHz, V_{FB} Resistor Programmed, 1.2V, 2A, Forced Continuous Mode

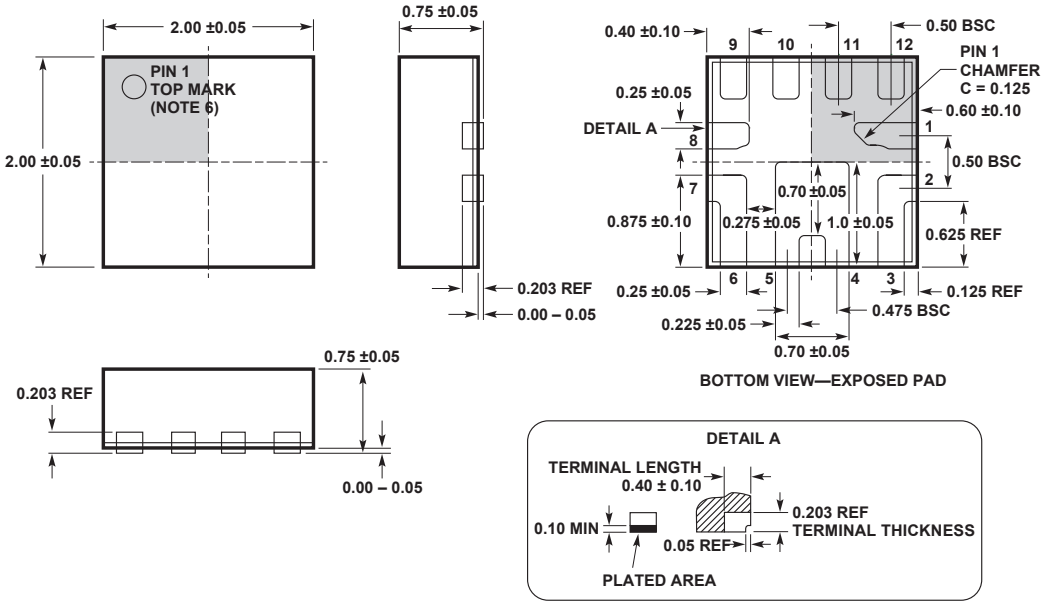


Fixed V_{OUT}, 0.5V, 2A, Burst Mode Operation

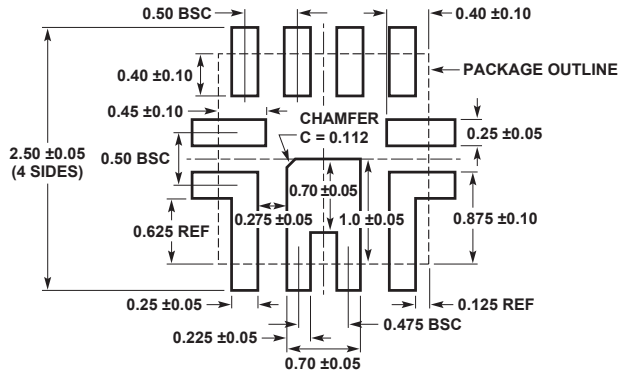


PACKAGE DESCRIPTION

UCM Package
12-Lead Plastic Side Solderable TQFN (2mm × 2mm)
(Reference DWG # 05-08-7072)



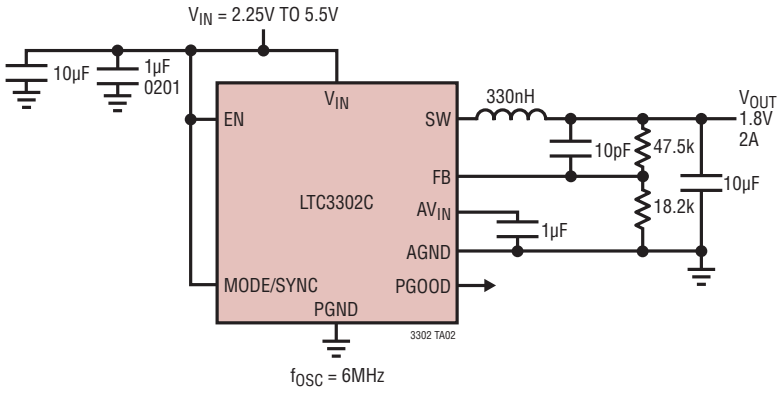
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

TYPICAL APPLICATION

6MHz, V_{FB} Resistor Programmed, 1.8V, 2A, Burst Mode Operation



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3307A	5V, 3A Synchronous Step-Down Silent Switcher in 2mm × 2mm LQFN	Monolithic Synchronous Step-Down DC/DC Capable of Supplying 3A at Switching Frequencies Up to 3MHz; Silent Switcher Architecture for Ultralow EMI Emissions; 2.25V to 5.5V Input Operating Range; 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy; PGOOD Indication, RT Programming, SYNC Input; 2mm × 2mm LQFN
LTC3308A	5V, 4A Synchronous Step-Down Silent Switcher in 2mm × 2mm LQFN	Monolithic Synchronous Step-Down DC/DC Capable of Supplying 4A at Switching Frequencies Up to 3MHz; Silent Switcher Architecture for Ultralow EMI Emissions; 2.25V to 5.5V Input Operating Range; 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy; PGOOD Indication, RT Programming, SYNC Input; 2mm × 2mm LQFN
LTC3310S	5V, 10A Synchronous Step-Down Silent Switcher 2 in 3mm × 3mm LQFN	Monolithic Synchronous Step-Down DC/DC Capable of Supplying 10A at Switching Frequencies Up to 5MHz; Silent Switcher Architecture for Ultralow EMI Emissions; 2.25V to 5.5V Input Operating Range; 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy; PGOOD Indication, RT Programming, SYNC Input; Configurable for Paralleling Power Stages; 3mm × 3mm LQFN
LTC3315A	Dual 5V, 2A Synchronous Step-Down DC/DCs in 2mm × 2mm LQFN	Dual Monolithic Synchronous Step-Down Voltage Regulators each Capable of Supplying 2A at Switching Frequencies up to 3MHz; 2.25V to 5.5V Input Operating Range; 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy; PGOOD Indication, SYNC Input; 2mm × 2mm LQFN
LTC3370/ LTC3371	4-Channel 8A Configurable 1A Buck DC/DCs	Four Synchronous Buck Regulators with 8 × 1A Power Stages; Can Connect Up to Four Power Stages in Parallel to Make a High Current Output (4A Maximum) with a Single Inductor, 8 Output Configurations Possible, Precision PGOOD Indication; LTC3371 Has a Watchdog Timer; LTC3370: 32-Lead 5mm × 5mm QFN; LTC3371: 38-Lead 5mm × 7mm QFN and TSSOP
LTC3374A	8-Channel Parallelable 1A Buck DC/DCs	Eight 1A Synchronous Buck Regulators; Can Connect Up to Four Power Stages in Parallel to Make a High Current Output (4A Maximum) with a Single Inductor, 15 Output Configurations Possible; Precision Enable Inputs and PGOOD_ALL Reporting; 38-Lead 5mm × 7mm QFN and TSSOP
LTC3375	8-Channel Parallelable 1A Buck DC/DCs	Eight 1A Synchronous Buck Regulators; Can Connect Up to Four Power Stages in Parallel to Make a High Current Output (4A Maximum) with a Single Inductor, 15 Output Configurations Possible; Precision Enable Inputs and PGOOD_ALL Reporting; I^2C Programming with a Watchdog Timer and Pushbutton; 48-Lead 7mm × 7mm QFN
LTC3412A	3A, 4MHz, Monolithic Synchronous Step-Down Regulator	95% Efficiency, V_{IN}: 2.25 to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 64µA, I_{SD} < 1µA, 4mm × 4mm QFN-16 Package
LTC3616	5.5V, 6A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25 to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 5mm QFN-24 Package