Embedded 56-pin Industrial Temperature Range CK505 Compatible Clock

ICS9ERS3125

Recommended Application:
Industrial temperature CK505-compatible clock

Output Features:
- 2 - CPU differential push-pull pairs
- 4 - SRC differential push-pull pairs
- 1 - CPU/SRC selectable differential push-pull pair
- 1 - DOT96/SRC selectable differential push-pull pair
- 1 - 27M/SRC/SE selectable pair
- 1 - SRC/SATA selectable differential push-pull pair
- 5 - PCI, 33MHz
- 1 - PCI_F 33MHz free running
- 1 - USB, 48MHz
- 1 - REF, 14.31818MHz

Key Specifications:
- CPU outputs cycle-cycle jitter < 85ps
- SRC output cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 250ps
- +/- 100ppm frequency accuracy on all outputs

Features/Benefits:
- Fully integrated Vreg
- Differential outputs have integrated series resistors to give Zo = 50 Ohms
- Supports spread spectrum modulation, 0 to -0.5% down spread
- Supports CPU clks up to 400MHz
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning

Table 1: CPU Frequency Select Table

<table>
<thead>
<tr>
<th>FS. C</th>
<th>FS. B</th>
<th>FS. A</th>
<th>CPU MHz</th>
<th>SRC MHz</th>
<th>PCI MHz</th>
<th>REF MHz</th>
<th>USB MHz</th>
<th>DOT MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>266.66</td>
<td>100.00</td>
<td>33.33</td>
<td>14.318</td>
<td>48.00</td>
<td>96.00</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>133.33</td>
<td>100.00</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>200.00</td>
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<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>166.66</td>
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<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>333.33</td>
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<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>100.00</td>
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<td>400.00</td>
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</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. FS. A and FS. B are low-threshold inputs. Please see VIL_FS and VIH_FS specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.
2. FS. C is a three-level input. Please see the VIL_FS and VIL_FS specifications in the Input/Supply/Common Output Parameters Table for correct values.

NOTE: Pin 23/24 defaults to a different spread domain than SRC without BIOS intervention.

CR # Control Table PCIEX pair control

<table>
<thead>
<tr>
<th>CR # SEL</th>
<th>SRC0 or SRC2</th>
<th>SRC1 or SRC4</th>
</tr>
</thead>
<tbody>
<tr>
<td>CR. RA</td>
<td>SRC0 or SRC2</td>
<td>SRC1 or SRC4</td>
</tr>
<tr>
<td>CR. BB</td>
<td>SRC0 or SRC2</td>
<td>SRC1 or SRC4</td>
</tr>
<tr>
<td>CR. RC</td>
<td>SRC0 or SRC2</td>
<td>SRC1 or SRC4</td>
</tr>
<tr>
<td>CR. RD</td>
<td>SRC1 or SRC4</td>
<td>SRC0 or SRC2</td>
</tr>
<tr>
<td>CR. RE</td>
<td>SRC0 or SRC2</td>
<td>SRC1 or SRC4</td>
</tr>
<tr>
<td>CR. RF</td>
<td>SRC0 or SRC2</td>
<td>SRC1 or SRC4</td>
</tr>
<tr>
<td>CR. RG</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>CR. RH</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

IDT™/ICS™ Embedded 56-Pin Industrial Temperature Range CK505 Compatible Clock

1612—08/19/09
## Pin Description

<table>
<thead>
<tr>
<th>PIN #</th>
<th>PIN NAME</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X2</td>
<td>OUT</td>
<td>Crystal output, nominally 14.318MHz.</td>
</tr>
<tr>
<td>2</td>
<td>X1</td>
<td>IN</td>
<td>Crystal input, Nominally 14.318MHz.</td>
</tr>
<tr>
<td>3</td>
<td>VDDREF</td>
<td>PWR</td>
<td>Power pin for the REF outputs, 3.3V nominal.</td>
</tr>
<tr>
<td>4</td>
<td>REF0/FSLC/TEST_SEL</td>
<td>I/O</td>
<td>3.3V 14.318MHz reference clock/3.3V tolerant low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values/ TEST_SEL: 3-level latched input to enable test mode. Refer to Test Clarification Table.</td>
</tr>
<tr>
<td>5</td>
<td>SDATA</td>
<td>I/O</td>
<td>Data pin for SMBus circuitry, 5V tolerant.</td>
</tr>
<tr>
<td>6</td>
<td>SCLK</td>
<td>IN</td>
<td>Clock pin of SMBus circuitry, 5V tolerant.</td>
</tr>
<tr>
<td>7</td>
<td>PCI0/CR#_A</td>
<td>I/O</td>
<td>3.3V PCI clock output/Clock Request control A for either SRC0 or SRC2 pair</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The power-up default is PCI0 output, but this pin may also be used as a Clock Request control of SRC pair 0 or SRC pair 2 via SMBus. Before configuring this pin as a Clock Request Pin, the PCI output must first be disabled in byte 2, bit 0 of SMBus address space. After the PCI output is disabled (high-Z), the pin can then be set to serve as a Clock Request pin for either SRC pair 0 or pair 2 by using the CR#_A_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 (default), 1 = CR#_A controls SRC2 pair.</td>
</tr>
<tr>
<td>8</td>
<td>VDDPCI</td>
<td>PWR</td>
<td>Power supply pin for the PCI outputs, 3.3V nominal.</td>
</tr>
<tr>
<td>9</td>
<td>PCI1/CR#_B</td>
<td>I/O</td>
<td>3.3V PCI clock output/Clock Request control B for either SRC1 or SRC4 pair</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The power-up default is PCI1 output, but this pin may also be used as a Clock Request control of SRC pair 1 or SRC pair 4 via SMBus. Before configuring this pin as a Clock Request Pin, the PCI output must first be disabled in byte 2, bit 1 of SMBus address space. After the PCI output is disabled (high-Z), the pin can then be set to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CR#_B_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 4 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default), 1 = CR#_B controls SRC4 pair.</td>
</tr>
<tr>
<td>10</td>
<td>PC12/TME</td>
<td>I/O</td>
<td>3.3V PCI clock output / Trusted Mode Enable (TME) Latched Input. This pin is sampled on power-up as follows 0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed After being sampled on power-up, this pin becomes a 3.3V PCI Output.</td>
</tr>
<tr>
<td>11</td>
<td>PCI3</td>
<td>OUT</td>
<td>3.3V PCI clock output.</td>
</tr>
<tr>
<td>12</td>
<td>PCI4/27_SEL</td>
<td>I/O</td>
<td>3.3V PCI clock output / 27MHz mode select for pin23, 24 strap. On powerup, the logic value on this pin determines the power-up default of DOT_96/SRC0 and 27MHz/LCD/SRC1 output and the function table for the pin23 and pin24.</td>
</tr>
<tr>
<td>13</td>
<td>PCI_F5/ITP_EN</td>
<td>I/O</td>
<td>Free running PCI clock output and ITP/SRC8 enable strap. This output is not affected by the state of the PCI_STOP# pin. On powerup, the state of this pin determines whether pins 45 and 46 are an ITP or SRC pair. 0 =SRC8/SRC8# 1 = ITP/ITP#</td>
</tr>
<tr>
<td>14</td>
<td>GNDPCI</td>
<td>PWR</td>
<td>Ground pin for PCI clocks.</td>
</tr>
<tr>
<td>15</td>
<td>VDD48</td>
<td>PWR</td>
<td>Power supply for USB clock, nominal 3.3V.</td>
</tr>
<tr>
<td>16</td>
<td>USB_48MHz/FSLA</td>
<td>I/O</td>
<td>Fixed 48MHz USB clock output, 3.3V / 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.</td>
</tr>
<tr>
<td>17</td>
<td>GND48</td>
<td>PWR</td>
<td>Ground pin for the 48MHz outputs.</td>
</tr>
<tr>
<td>18</td>
<td>VDD96.IO</td>
<td>PWR</td>
<td>Power supply for DOT96 output, 1.05 to 3.3V +/-5%.</td>
</tr>
<tr>
<td>19</td>
<td>DOTT_96/SRCT0</td>
<td>OUT</td>
<td>True clock of SRC or DOT96. The power-up default function is SRC0. After powerup, this pin function may be changed to DOT96 via SMBus Byte 1, bit 7 as follows: 0= SRC0 1=DOT96</td>
</tr>
<tr>
<td>20</td>
<td>DOTC_96/SRCC0</td>
<td>OUT</td>
<td>Complement clock of SRC or DOT96. The power-up default function is SRC0#. After powerup, this pin function may be changed to DOT96# via SMBus Byte 1, bit 7 as follows: 0= SRC0# 1=DOT96#</td>
</tr>
<tr>
<td>Pin</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-----</td>
<td>-------------------------------------------------------------------------------------------------------</td>
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<td></td>
</tr>
<tr>
<td>21</td>
<td>GND</td>
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<td></td>
</tr>
<tr>
<td>22</td>
<td>VDD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>27FIX/LCDT/SRCT_L1/SE1 OUT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>27SS/LCDC/SRCC_L1/SE2 OUT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>GND</td>
<td></td>
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</tr>
<tr>
<td>26</td>
<td>VDDPLL3_IO</td>
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</tr>
<tr>
<td>27</td>
<td>SRCT2/SATAT OUT</td>
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<td></td>
</tr>
<tr>
<td>28</td>
<td>SRCC2/SATAC OUT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>GNDSRC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>SRCT3/CR#_C</td>
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<td></td>
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<td>SRCC3/CR#_D</td>
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<td>VDDSRC_IO</td>
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<td>35</td>
<td>GNDSRC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>SRCC11/CR#_G</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Pin Description (continued)**

- **23 27FIX/LCDT/SRCT_L1/SE1 OUT**
  - Single-ended 3.3V 27MHz fx clock output / True clock of differential SRC1 or LCD clock pair / Single ended 3.3V peripheral clock output. The default output selection is determined by the SEL_27 default latch value. See below:
  1. **SEL_27=0**: LCD100 with -0.5% down spread is selected as default. LCD100 spread percentage can be adjusted OR output can be changed to SRC or 3.3V single-ended peripheral clock output via SMBUs B1b[4:1].
  2. **SEL_27=1**: Single-ended 27MHz output is selected.

- **24 27SS/LCDC/SRCC_L1/SE2 OUT**
  - Single-ended 3.3V 27MHz fix clock output / Complementary clock of differential SRC1 or LCD clock pair / Single ended 3.3V peripheral clock output. The default output selection is determined by the SEL_27 default latch value. See below:
  1. **SEL_27=0**: LCD100 with -0.5% down spread is selected as default. LCD100 spread percentage can be adjusted OR output can be changed to SRC or 3.3V single-ended peripheral clock output via SMBUs B1b[4:1].
  2. **SEL_27=1**: Single-ended 27SS output is selected with -0.5% down spread as default. Spread percentage can be adjusted via SMBus B1b[4:1].

- **30 SRCT3/CR#_C I/O**
  - True clock of differential SRC clock pair / Clock Request control C for either SRC0 or SRC2 pair
  - The power-up default is SRCCCLK3 output, but this pin may also be used as a Clock Request control of SRC pair 0 or SRC pair 2 via SMBus. Before configuring this pin as a Clock Request pin, the SRC3 output must first be disabled in byte 4, bit 7 of SMBus address space.
  - After the SRC3 output is disabled, the pin can then be set to serve as a Clock Request pin for either SRC pair 2 or pair 0 using the CR#_C_EN bit located in byte 5 of SMBus address space.
  - **Byte 5, bit 3**
  1. **0**: SRC3 enabled (default)
  2. **1**: CR#_C enabled.
  - **Byte 5, bit 2**
  1. **0**: CR#_C controls SRC0 pair (default),
  2. **1**: CR#_C controls SRC2 pair.

- **31 SRCC3/CR#_D I/O**
  - Complementary clock of differential SRC clock pair / Clock Request control D for either SRC1 or SRC4 pair
  - The power-up default is SRCCCLK3 output, but this pin may also be used as a Clock Request control of SRC pair 1 or SRC pair 4 via SMBus. Before configuring this pin as a Clock Request pin, the SRC3 output must first be disabled in byte 4, bit 7 of SMBus address space.
  - After the SRC3 output is disabled, the pin can then be set to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CR#_D_EN bit located in byte 5 of SMBus address space.
  - **Byte 5, bit 1**
  1. **0**: SRC3 enabled (default)
  2. **1**: CR#_D enabled.
  - **Byte 5, bit 0**
  1. **0**: CR#_D controls SRC1 pair (default),
  2. **1**: CR#_D controls SRC4 pair.

- **32 VDDSRC_IO PWR**
  - Power supply for SRC clocks. 1.05 to 3.3V +/-5%.

- **33 SRCT4 I/O**
  - True clock of differential SRC clock pair 4

- **34 SRCC4 I/O**
  - Complement clock of differential SRC clock pair 4

- **35 GNDSRC PWR**
  - Ground for SRC clocks

- **36 SRCC11/CR#_G I/O**
  - SRC11 complement /Clock Request control for SRC10 pair
  - The power-up default is SRC11#, but this pin may also be used as a Clock Request control of SRC10 via SMBus. Before configuring this pin as a Clock Request pin, the SRC11 output pair must first be disabled in byte 3, bit 7 of SMBus configuration space. After the SRC11 output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC10 pair using byte 6, bit 5 of SMBus configuration space.
  - **Byte 6, bit 5**
  1. **0**: SRC11# enabled (default)
  2. **1**: CR#_G controls SRC10

**NOTE:** SRC10 NOT AVAILABLE ON 9LRS312S
### Pin Description (continued)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
</table>
| 37  | SRCT11/CR#_H | I/O  | SRCT1 true or Clock Request control H for SRC11 pair. The power-up default is SRC11, but this pin may also be used as a Clock Request control of SRC3 via SMBus. Before configuring this pin as a Clock Request Pin, the SRCT11 output pair must first be disabled in byte 3, bit 7 of SMBus configuration space. After the SRC11 output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC3 pair using byte 6, bit 4 of SMBus configuration space. Byte 6, bit 4  
0 = SRC11 enabled (default)  
1 = CR#_H controls SRC3.  
**NOTE:** SRC10 not available on 9LRS3125. |
| 38  | VDDSRC_IO   | PWR  | Power supply for SRC outputs. 1.05 to 3.3V +/-5%. |
| 39  | CPU_STOP#   | IN   | Stops all CPU Clocks, except those set to be free running clocks. In AMT mode 3 bits are shifted in from the ICH to set the FSC, FSB, FSA values. |
| 40  | PCI_STOP#   | IN   | Stops all PCI/SRC Clocks, except those set to be free running clocks. In AMT mode, this pin is a clock input which times the FSC, FSB, FSA bits shifted in on CPU_STOP#. |
| 41  | VDDSRC     | PWR  | 3.3V Power supply for SRC PLL and Logic. |
| 42  | GNDSRC     | PWR  | Ground for SRC clocks. |
| 43  | SRCC7CR#_E | I/O  | SRC7 complement or Clock Request control E for SRC8 pair. The power-up default is SRC7#, but this pin may also be used as a Clock Request control of SRC7 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC7 output pair must first be disabled in byte 3, bit 3 of SMBus configuration space. After the SRC output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC8 pair using byte 6, bit 6 of SMBus configuration space. Byte 6, bit 6  
0 = SRC7# enabled (default)  
1 = CR#_E controls SRC8. |
| 44  | SRCT7/CR#_F | I/O  | SRC7 true or Clock Request control 8 for SRC8 pair. The power-up default is SRC7#, but this pin may also be used as a Clock Request control of SRC7 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC7 output pair must first be disabled in byte 3, bit 3 of SMBus configuration space. After the SRC output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC8 pair using byte 6, bit 6 of SMBus configuration space. Byte 6, bit 6  
0 = SRC7# enabled (default)  
1 = CR#_F controls SRC8. |
| 45  | CPUC2_ITP/SRCC8 | OUT | Complement clock of low power differential CPU2/Complement clock of differential SRC pair. The function of this pin is determined by the latched input value on pin 14, PCIF5/ITP_EN on powerup. The function is as follows:  
Pin 14 latched input Value  
0 = SRC8#  
1 = ITP#. |
| 46  | CPUT2_ITP/SRCT8 | OUT | True clock of low power differential CPU2/True clock of differential SRC pair. The function of this pin is determined by the latched input value on pin 14, PCIF5/ITP_EN on powerup. The function is as follows:  
Pin 14 latched input Value  
0 = SRC8  
1 = ITP. |
| 47  | VDDCPU/O    | PWR  | Power supply for CPU outputs. 1.05 to 3.3V +/-5%. |
| 48  | CPUC1_F     | OUT  | Complement clock of low power differential CPU clock pair. This clock will be free-running during iAMT. |
| 49  | CPUT1_F     | OUT  | True clock of low power differential CPU clock pair. This clock will be free-running during iAMT. |
| 50  | GNDCPU      | PWR  | Ground Pin for CPU Outputs. |
| 51  | CPU0        | OUT  | Complement clock of low power differential CPU clock pair. |
| 52  | CPUT0        | OUT  | True clock of low power differential CPU clock pair. |
| 53  | VDDCPU      | PWR  | 3.3V Power Supply for CPU. |
| 54  | CK_PWRGD/PD# | IN   | Notifies CK505 to sample latched inputs, or iAMT entry/exit, or PWRDWN# mode. |
| 55  | FSLB/TEST_MODE | IN | 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for VI_FS and Vih_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. |
| 56  | GNDREF      | PWR  | Ground pin for crystal oscillator circuit. |
General Description

**ICS9ERS3125** is electrically compliant to the Intel CK505 Yellow Cover specification. This clock synthesizer provides a single chip solution for Intel chipsets. **ICS9ERS3125** is driven with a 14.318MHz crystal.

### Block Diagram

![Block Diagram](image)

### Power Groups

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>VDD</th>
<th>GND</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>47</td>
<td>50</td>
<td>50</td>
<td>CPUCLK</td>
</tr>
<tr>
<td>53</td>
<td>50</td>
<td></td>
<td>Master Clock, Analog</td>
</tr>
<tr>
<td>26, 32, 38</td>
<td>29, 35, 42</td>
<td>27SS - SE2, LCD/SRC1</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>42</td>
<td></td>
<td>SRCCLK</td>
</tr>
<tr>
<td>26</td>
<td>25</td>
<td></td>
<td>PLL2</td>
</tr>
<tr>
<td>22</td>
<td>25</td>
<td></td>
<td>PLL1/SE</td>
</tr>
<tr>
<td>18</td>
<td>21</td>
<td></td>
<td>DOT 96Mhz</td>
</tr>
<tr>
<td>15</td>
<td>17</td>
<td></td>
<td>USB 48 output and PLL</td>
</tr>
<tr>
<td>3</td>
<td>56</td>
<td></td>
<td>Xtal, REF</td>
</tr>
<tr>
<td>8</td>
<td>14</td>
<td></td>
<td>PCICLK</td>
</tr>
</tbody>
</table>

**IDT™/ICS™** Embedded 56-Pin Industrial Temperature Range CK505 Compatible Clock

1612—08/19/09
Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Supply Voltage</td>
<td>VDDxxx</td>
<td>Supply Voltage</td>
<td>4.6</td>
<td>V</td>
<td>1,7</td>
<td></td>
</tr>
<tr>
<td>Maximum Supply Voltage</td>
<td>VDDxxx_IO</td>
<td>Low-Voltage Differential I/O Supply</td>
<td>3.8</td>
<td>V</td>
<td>1,7</td>
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<tr>
<td>Maximum Input Voltage</td>
<td>VIH</td>
<td>3.3V LVCMOS Inputs</td>
<td>4.6</td>
<td>V</td>
<td>1,7,8</td>
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<tr>
<td>Minimum Input Voltage</td>
<td>VIL</td>
<td>Any Input</td>
<td>GND - 0.5</td>
<td>V</td>
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<tr>
<td>Storage Temperature</td>
<td>Ts</td>
<td>-</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
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<tr>
<td>Case Temperature</td>
<td>Tcase</td>
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<td>115</td>
<td>°C</td>
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<tr>
<td>Input ESD protection</td>
<td>ESD prot</td>
<td>Human Body Model</td>
<td>2000</td>
<td>V</td>
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Electrical Characteristics - Input/Supply/Common Output Parameters

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<td>Tambient</td>
<td>-</td>
<td>-40</td>
<td>85</td>
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<td>Supply Voltage</td>
<td>VDDxxx</td>
<td>Supply Voltage</td>
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<td>3.465</td>
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<td>Supply Voltage</td>
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<td>V</td>
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<tr>
<td>Input High Voltage</td>
<td>VINSE</td>
<td>Single-ended inputs</td>
<td>2</td>
<td>VDD + 0.3</td>
<td>V</td>
<td>1</td>
<td></td>
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<tr>
<td>Input Low Voltage</td>
<td>VILSE</td>
<td>Single-ended inputs</td>
<td>VSS + 0.3</td>
<td>0.8</td>
<td>V</td>
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<tr>
<td>Input Leakage Current</td>
<td>IIN</td>
<td></td>
<td>-5</td>
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<td>μA</td>
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<td>Input Leakage Current</td>
<td>IINRES</td>
<td>Inputs with pull or pull down resistors</td>
<td>-200</td>
<td>200</td>
<td>μA</td>
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<tr>
<td>Output High Voltage</td>
<td>VOHSE</td>
<td>Single-ended outputs, IOH = -1mA</td>
<td>2.4</td>
<td>V</td>
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<td>Output Low Voltage</td>
<td>VOLSE</td>
<td>Single-ended outputs, IOL = 1 mA</td>
<td>0.4</td>
<td>V</td>
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<td>Output High Voltage</td>
<td>VOHDF</td>
<td>Differential Outputs</td>
<td>0.7</td>
<td>0.9</td>
<td>V</td>
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<td>Output Low Voltage</td>
<td>VOLDF</td>
<td>Differential Outputs</td>
<td>0.4</td>
<td>V</td>
<td>1</td>
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<td>Low Threshold Input-High Voltage (Test Mode)</td>
<td>VIH_FS_TEST</td>
<td>3.3 V +/-5%</td>
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<td>VDD + 0.3</td>
<td>V</td>
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<tr>
<td>Low Threshold Input-High Voltage</td>
<td>VIH_Fs</td>
<td>3.3 V +/-5%</td>
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<td>1.5</td>
<td>V</td>
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<tr>
<td>Low Threshold Input-Low Voltage</td>
<td>VIL_Fs</td>
<td>3.3 V +/-5%</td>
<td>VSS + 0.3</td>
<td>0.35</td>
<td>V</td>
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<td>Operating Supply Current</td>
<td>IDD_DEFAULT</td>
<td>3.3V supply, PLL1,2 off</td>
<td>95</td>
<td>125</td>
<td>mA</td>
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<td></td>
<td>IDD_PLL1</td>
<td>3.3V supply, PLL1,2 Differential Out</td>
<td>106</td>
<td>125</td>
<td>mA</td>
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<td></td>
<td>IDD_PLL2</td>
<td>3.3V supply, PLL1,2 Single-ended Out</td>
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<td>125</td>
<td>mA</td>
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<td></td>
<td>IDD_PLL3</td>
<td>0.8V supply, Differential I/O current, all outputs enabled</td>
<td>25</td>
<td>32</td>
<td>50</td>
<td>mA</td>
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<tr>
<td>Power Down Current</td>
<td>IDD_PD3</td>
<td>3.3V supply, Power Down Mode</td>
<td>26</td>
<td>30</td>
<td>mA</td>
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<td></td>
<td>IDD_PDI0</td>
<td>0.8V IO supply, Power Down Mode</td>
<td>0.23</td>
<td>0.5</td>
<td>mA</td>
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<tr>
<td>iAMT Mode Current</td>
<td>IDD_IAMT3</td>
<td>3.3V supply, iAMT Mode</td>
<td>47</td>
<td>60</td>
<td>mA</td>
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<td></td>
<td>IDD_IAMT0</td>
<td>0.8V IO supply, iAMT Mode</td>
<td>5</td>
<td>10</td>
<td>mA</td>
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<tr>
<td>Input Frequency</td>
<td>F_i</td>
<td>VDD = 3.3 V</td>
<td>14.318</td>
<td>MHz</td>
<td>2</td>
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<td>Pin Inductance</td>
<td>L_pin</td>
<td></td>
<td>7</td>
<td>nH</td>
<td>1</td>
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<tr>
<td>Input Capacitance</td>
<td>Cin</td>
<td>Logic Inputs</td>
<td>1.5</td>
<td>5</td>
<td>pF</td>
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<td></td>
<td>Cout</td>
<td>Output pin capacitance</td>
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<td>pF</td>
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<tr>
<td></td>
<td>CNX</td>
<td>X1 &amp; X2 pins</td>
<td>5</td>
<td>pF</td>
<td>1</td>
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<tr>
<td>Spread Spectrum Modulation Frequency</td>
<td>fSSMOD</td>
<td>Triangular Modulation</td>
<td>30</td>
<td>33</td>
<td>kHz</td>
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# Electrical Characteristics - SMBus Interface

<table>
<thead>
<tr>
<th>PARAMETER</th>
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<tbody>
<tr>
<td>SMBus Voltage</td>
<td>VDD</td>
<td></td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
<td>1</td>
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<tr>
<td>Low-level Output Voltage</td>
<td>V_{OLSMB}</td>
<td>@ I_{FULLUP}</td>
<td></td>
<td>0.4</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Current sinking at V_{OLSMB} = 0.4 V</td>
<td>I_{FULLUP}</td>
<td>SMB Data Pin</td>
<td>4</td>
<td></td>
<td>mA</td>
<td>1</td>
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<tr>
<td>SCLK/SDATA Clock/Data Rise Time</td>
<td>T_{RDC}</td>
<td>(Max VIL - 0.15) to (Min VIH + 0.15)</td>
<td>1000</td>
<td>ns</td>
<td></td>
<td>1</td>
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<tr>
<td>SCLK/SDATA Clock/Data Fall Time</td>
<td>T_{FDC}</td>
<td>(Min VIH + 0.15) to (Max VIL - 0.15)</td>
<td>300</td>
<td>ns</td>
<td></td>
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<tr>
<td>Maximum SMBus Operating Frequency</td>
<td>F_{SMBUS}</td>
<td>Block Mode</td>
<td>100</td>
<td>kHz</td>
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# AC Electrical Characteristics - Input/Common Parameters

<table>
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<tr>
<td>Clk Stabilization</td>
<td>T_{STAB}</td>
<td>From VDD Power-Up or de-assertion of PD# to 1st clock</td>
<td>1.8</td>
<td>ms</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Tdrive_SRC</td>
<td>T_{DRSRC}</td>
<td>SRC output enable after PCI_STOP# de-assertion</td>
<td>15</td>
<td>ns</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Tdrive_PD#</td>
<td>T_{DRPD}</td>
<td>Differential output enable after PD# de-assertion</td>
<td>300</td>
<td>us</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Tdrive_CPU</td>
<td>T_{DRSRC}</td>
<td>CPU output enable after CPU_STOP# de-assertion</td>
<td>10</td>
<td>ns</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Tfall_PD#</td>
<td>T_{FALL}</td>
<td>Fall/rise time of PD#, PCI_STOP# and CPU_STOP# inputs</td>
<td>5</td>
<td>ns</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Trise_PD#</td>
<td>T_{RISE}</td>
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<td>5</td>
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# AC Electrical Characteristics - Low Power Differential Outputs

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<th>MAX</th>
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<th>NOTES</th>
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</thead>
<tbody>
<tr>
<td>Rising Edge Slew Rate</td>
<td>t_{SLR}</td>
<td>Differential Measurement</td>
<td>2.5</td>
<td>8</td>
<td>V/μs</td>
<td>1,2</td>
</tr>
<tr>
<td>Falling Edge Slew Rate</td>
<td>t_{FLR}</td>
<td>Differential Measurement</td>
<td>2.5</td>
<td>8</td>
<td>V/μs</td>
<td>1,2</td>
</tr>
<tr>
<td>Slew Rate Variation</td>
<td>t_{SLVAR}</td>
<td>Single-ended Measurement</td>
<td>20</td>
<td>%</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Maximum Output Voltage</td>
<td>V_{HIGH}</td>
<td>Includes overshoot</td>
<td>1150</td>
<td>mV</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Minimum Output Voltage</td>
<td>V_{LOW}</td>
<td>Includes undershoot</td>
<td>-300</td>
<td>mV</td>
<td>1</td>
<td>1</td>
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<td>Differential Voltage Swing</td>
<td>V_{SWING}</td>
<td>Differential Measurement</td>
<td>300</td>
<td>mV</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Crossing Point Voltage</td>
<td>V_{XABS}</td>
<td>Single-ended Measurement</td>
<td>300</td>
<td>mV</td>
<td>550</td>
<td>1,3,4</td>
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<tr>
<td>Crossing Point Variation</td>
<td>V_{XABSVAR}</td>
<td>Single-ended Measurement</td>
<td>140</td>
<td>mV</td>
<td>1,3,5</td>
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<tr>
<td>Duty Cycle</td>
<td>D_{CYC}</td>
<td>Differential Measurement</td>
<td>45</td>
<td>%</td>
<td>1</td>
<td>1</td>
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<tr>
<td>CPU Jitter - Cycle to Cycle</td>
<td>CPUJ_{C2C}</td>
<td>Differential Measurement</td>
<td>85</td>
<td>ps</td>
<td>1</td>
<td>1</td>
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<tr>
<td>SRC Jitter - Cycle to Cycle</td>
<td>SRCJ_{C2C}</td>
<td>Differential Measurement</td>
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<td>ps</td>
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<td>SATA Jitter - Cycle to Cycle</td>
<td>SATAJ_{C2C}</td>
<td>Differential Measurement</td>
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<td>DOT Jitter - Cycle to Cycle</td>
<td>DOTJ_{C2C}</td>
<td>Differential Measurement</td>
<td>250</td>
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<tr>
<td>CPU[1:0] Skew</td>
<td>CPU_{SKEW10}</td>
<td>Differential Measurement</td>
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<td>ps</td>
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<td>CPU[2:1:ITP:0] Skew</td>
<td>CPU_{SKEW20}</td>
<td>Differential Measurement</td>
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<td>ps</td>
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<tr>
<td>SRC[11,7,4,2,0] Skew</td>
<td>SRC_{SKEW}</td>
<td>Differential Measurement</td>
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<td>ps</td>
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<td>SRC[11:0] Skew</td>
<td>SRC_{SKEW}</td>
<td>Differential Measurement</td>
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*TA = -40 - 85°C; Supply Voltage VDD = 3.3 V +/-5%, Rs= 0Ω, CL = 2pF
### Electrical Characteristics - PCICLK/PCICLK_F

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<tr>
<td>Long Accuracy</td>
<td>ppm</td>
<td>see Tperiod min-max values</td>
<td>-100</td>
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<td>ppm</td>
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<tr>
<td>Clock period</td>
<td>T_period</td>
<td>33.33MHz output nominal</td>
<td>29.99718</td>
<td>30.50300</td>
<td>ns</td>
<td>6</td>
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<tr>
<td>Absolute min/max period</td>
<td>T_abs</td>
<td>33.33MHz output nominal/spread</td>
<td>29.49718</td>
<td>30.65320</td>
<td>ns</td>
<td>6</td>
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<tr>
<td>Output High Voltage</td>
<td>V_OH</td>
<td>V_OH @ MIN = 1.0 V</td>
<td>-33</td>
<td>-33</td>
<td>mA</td>
<td>1</td>
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<tr>
<td>Output Low Voltage</td>
<td>V_CL</td>
<td>I_CL = 1 mA</td>
<td>0.4</td>
<td>0.4</td>
<td>V</td>
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<tr>
<td>Output Current</td>
<td>I_OH</td>
<td>V_OH @ MIN = 1.0 V</td>
<td>30</td>
<td>38</td>
<td>mA</td>
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<td>Rising Edge Slew Rate</td>
<td>t_SLR</td>
<td>Measured from 0.8 to 2.0 V</td>
<td>1</td>
<td>4</td>
<td>V/ns</td>
<td>1</td>
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<tr>
<td>Falling Edge Slew Rate</td>
<td>t_FLR</td>
<td>Measured from 2.0 to 0.8 V</td>
<td>1</td>
<td>4</td>
<td>V/ns</td>
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<tr>
<td>Duty Cycle</td>
<td>d_1</td>
<td>V_T = 1.5 V</td>
<td>45</td>
<td>55</td>
<td>%</td>
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<tr>
<td>Jitter, Cycle to cycle</td>
<td>t_delay</td>
<td>V_T = 1.5 V</td>
<td>200</td>
<td>500</td>
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*TA = -40 - 85°C; Supply Voltage VDD = 3.3 V +/-5%; Rs = 39Ω, CL = 5pF

### Electrical Characteristics - USB48MHz

<table>
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<th>CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
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<tr>
<td>Long Accuracy</td>
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<td>see Tperiod min-max values</td>
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<td>ppm</td>
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<td>Clock period</td>
<td>T_period</td>
<td>48.00MHz output nominal</td>
<td>20.83125</td>
<td>20.83542</td>
<td>ns</td>
<td>6</td>
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<td>Absolute min/max period</td>
<td>T_abs</td>
<td>48.00MHz output nominal</td>
<td>20.13125</td>
<td>21.53542</td>
<td>ns</td>
<td>6</td>
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<tr>
<td>Output High Voltage</td>
<td>V_OH</td>
<td>V_OH @ MIN = 1.0 V</td>
<td>-29</td>
<td>-23</td>
<td>mA</td>
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<tr>
<td>Output Low Voltage</td>
<td>V_CL</td>
<td>I_CL = 1 mA</td>
<td>0.4</td>
<td>0.4</td>
<td>V</td>
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<tr>
<td>Rising Edge Slew Rate</td>
<td>t_SLR</td>
<td>Measured from 0.8 to 2.0 V</td>
<td>1</td>
<td>2</td>
<td>V/ns</td>
<td>1</td>
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<tr>
<td>Falling Edge Slew Rate</td>
<td>t_FLR</td>
<td>Measured from 2.0 to 0.8 V</td>
<td>1</td>
<td>2</td>
<td>V/ns</td>
<td>1</td>
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<tr>
<td>Duty Cycle</td>
<td>d_1</td>
<td>V_T = 1.5 V</td>
<td>45</td>
<td>55</td>
<td>%</td>
<td>1</td>
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<tr>
<td>Jitter, Cycle to cycle</td>
<td>t_delay</td>
<td>V_T = 1.5 V</td>
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<td>350</td>
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*TA = -40 - 85°C; Supply Voltage VDD = 3.3 V +/-5%; Rs = 39Ω, CL = 5pF

### Electrical Characteristics - REF-14.318MHz

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>Notes</th>
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<tbody>
<tr>
<td>Long Accuracy</td>
<td>ppm</td>
<td>see Tperiod min-max values</td>
<td>-100</td>
<td>100</td>
<td>ppm</td>
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<tr>
<td>Clock period</td>
<td>T_period</td>
<td>14.318MHz output nominal</td>
<td>69.8343</td>
<td>69.8483</td>
<td>ns</td>
<td>6</td>
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<tr>
<td>Absolute min/max period</td>
<td>T_abs</td>
<td>14.318MHz output nominal</td>
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<td>70.84825</td>
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<tr>
<td>Output High Voltage</td>
<td>V_OH</td>
<td>V_OH @ MIN = 1.0 V</td>
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<td>-33</td>
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<tr>
<td>Output Low Voltage</td>
<td>V_CL</td>
<td>I_CL = 1 mA</td>
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<td>0.4</td>
<td>V</td>
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<tr>
<td>Rising Edge Slew Rate</td>
<td>t_SLR</td>
<td>Measured from 0.8 to 2.0 V</td>
<td>1</td>
<td>4</td>
<td>V/ns</td>
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<tr>
<td>Falling Edge Slew Rate</td>
<td>t_FLR</td>
<td>Measured from 2.0 to 0.8 V</td>
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<td>4</td>
<td>V/ns</td>
<td>1</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>d_1</td>
<td>V_T = 1.5 V</td>
<td>45</td>
<td>55</td>
<td>%</td>
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<tr>
<td>Jitter, Cycle to cycle</td>
<td>t_delay</td>
<td>V_T = 1.5 V</td>
<td>1000</td>
<td>1000</td>
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*TA = -40 - 85°C; Supply Voltage VDD = 3.3 V +/-5%; Rs = 39Ω, CL = 5pF
Electrical Characteristics - 27MHz_Spread / 27MHz_NonSpread

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<tr>
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<th>SYMBOL</th>
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<th>MAX</th>
<th>UNITS</th>
<th>Notes</th>
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<td>ppm</td>
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<td>T_period</td>
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<td>I_CHI = -1 mA</td>
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<td>V</td>
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<td>Output Low Voltage</td>
<td>V_CL</td>
<td>I_CL = 1 mA</td>
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<td>V</td>
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<td>Output High Current</td>
<td>I_OH</td>
<td>V_CH @ MIN = 1.0 V</td>
<td>-29</td>
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<td>mA</td>
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<td></td>
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<td>V_CH @ MAX = 3.135 V</td>
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<td>Output Low Current</td>
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<td>V_CL @ MIN = 1.95 V</td>
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<td></td>
<td>V_CL @ MAX = 0.4 V</td>
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<td>mA</td>
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<td>Edge Rate</td>
<td>t slew</td>
<td>Rising/Falling edge rate</td>
<td>1</td>
<td>4</td>
<td>V/ns</td>
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</tr>
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<td>Rise Time</td>
<td>t_r</td>
<td>V_C = 0.4 V, V_CH = 2.4 V</td>
<td>0.5</td>
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<tr>
<td>Fall Time</td>
<td>t_f</td>
<td>V_CH = 2.4 V, V_CL = 0.4 V</td>
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<td>ns</td>
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<tr>
<td>Duty Cycle</td>
<td>d_t</td>
<td>V_T = 1.5 V</td>
<td>45</td>
<td>55</td>
<td>%</td>
<td>1</td>
</tr>
<tr>
<td>Jitter</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>t_j</td>
<td>Long Term (10us), VT = 1.5 V</td>
<td>800</td>
<td></td>
<td>ps</td>
<td>1</td>
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<tr>
<td></td>
<td>t_j(PCI)</td>
<td>V_T = 1.5 V</td>
<td>-200</td>
<td>200</td>
<td>ps</td>
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<tr>
<td></td>
<td>t_j(Cyc-Cyc)</td>
<td>V_T = 1.5 V</td>
<td></td>
<td></td>
<td>ps</td>
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*TA = -40 - 85°C; Supply Voltage VDD = 3.3 V +/-5%, Rs = 39Ω, CL = 5pF

Electrical Characteristics - Differential Jitter Parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>TYP</th>
<th>Max</th>
<th>Units</th>
<th>Notes</th>
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</thead>
<tbody>
<tr>
<td>Jitter, Phase</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td>t_phasePLL</td>
<td>PCIe Gen 1</td>
<td>86</td>
<td></td>
<td></td>
<td>ps (p-p)</td>
<td>1,11</td>
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<td>t_phaseLo</td>
<td>PCIe Gen 2</td>
<td>3</td>
<td></td>
<td></td>
<td>ps (RMS)</td>
<td>1,11</td>
</tr>
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<td></td>
<td>PCIe Gen 2</td>
<td></td>
<td></td>
<td></td>
<td>ps (RMS)</td>
<td>1,11</td>
</tr>
</tbody>
</table>

*TA = -40 - 85°C; Supply Voltage VDD = 3.3 V +/-5%, Rs= 0Ω, CL = 2pF

Notes on Electrical Characteristics:

1Guaranteed by design and characterization, not 100% tested in production.
2Slew rate measured through Vswing centered around differential zero
3Vxabs is defined as the voltage where CLK = CLK#
4Only applies to the differential rising edge (CLK rising and CLK# falling)
5Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.
6The average cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.
7All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz
8Operation under these conditions is neither implied, nor guaranteed.
9Maximum input voltage is not to exceed maximum VDD
10See PCI Clock-to-Clock Delay Figure
11See http://www.pcisig.com for complete specs
### Table 1: CPU Frequency Select Table

<table>
<thead>
<tr>
<th>FS_L²</th>
<th>FS_H¹ B₀b₆</th>
<th>FS_H¹ B₀b₅</th>
<th>CPU MHz</th>
<th>SRC MHz</th>
<th>PCI MHz</th>
<th>REF MHz</th>
<th>USB MHz</th>
<th>DOT MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>0 0</td>
<td>266.66</td>
<td>100.00</td>
<td>100.00</td>
<td>133.33</td>
<td>48.00</td>
<td>96.00</td>
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<tr>
<td>0 0</td>
<td>0 1</td>
<td>133.33</td>
<td></td>
<td></td>
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<td>100.00</td>
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</tbody>
</table>

1. FS_H¹ and FS_L² are low-threshold inputs. Please see $V_{IL,FS}$ and $V_{IH,FS}$ specifications in the Input/Supply/Common Output Parameters Table for correct values.

Also refer to the Test Clarification Table.

2. FS_L³ is a three-level input. Please see the $V_{IL,FS}$ and $V_{IH,FS}$ specifications in the Input/Supply/Common Output Parameters Table for correct values.

### Table 2: 27FIX/LCDT/SRCT_LR1/SE1, 27SS/LCDC/SRCC_LR1/SE2 Configuration

<table>
<thead>
<tr>
<th>27_SEL</th>
<th>B₁b₄</th>
<th>B₁b₃</th>
<th>B₁b₂</th>
<th>B₁b₁</th>
<th>27FIX/LCDT/SRCT_LR1/SE1</th>
<th>27SS/LCDC/SRCC_LR1/SE2</th>
<th>Spread MHz</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0</td>
<td>0 0 0 0</td>
<td>100.00</td>
<td>PLL1 &amp; PLL2 disabled</td>
<td>SRCLK1 from SRC_MAIN</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 0 0</td>
<td>0 0 0 1</td>
<td>100.00</td>
<td>100.00</td>
<td>-0.50%</td>
<td></td>
<td>LCDCLK from PLL1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 0 0</td>
<td>0 0 1 1</td>
<td>100.00</td>
<td>100.00</td>
<td>-1%</td>
<td></td>
<td>LCDCLK from PLL1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 0 0</td>
<td>0 1 0 0</td>
<td>100.00</td>
<td>100.00</td>
<td>-1.50%</td>
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<td>LCDCLK from PLL1</td>
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<tr>
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<td>0 1 0 1</td>
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<td>100.00</td>
<td>+/-0.25%</td>
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<td>LCDCLK from PLL1</td>
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<td>100.00</td>
<td>+0.5%</td>
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<tr>
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<td>100.00</td>
<td>+/-0.5%</td>
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<td>LCDCLK from PLL1</td>
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<td>24.576 Mhz on SE1 and SE2</td>
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Note: Mode 00000 – 00110 on Table 2 only applies when SRC_MAIN source is from PLL5.
### Table 3: IO_Vout select table

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</tr>
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### Table 4: Device ID table

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<th>B8b6</th>
<th>B8b5</th>
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<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
### CPU Power Management Table

<table>
<thead>
<tr>
<th>PD#</th>
<th>CPU_STOP#</th>
<th>PCI_STOP#</th>
<th>PEREQ#</th>
<th>SMBus Register OE</th>
<th>CPU0</th>
<th>CPU0#</th>
<th>CPU1</th>
<th>CPU1#</th>
<th>CPU2</th>
<th>CPU2#</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>X</td>
<td>Enable</td>
<td>Running</td>
<td>Running</td>
<td>Running</td>
<td>Running</td>
<td>Running</td>
<td>Running</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Enable</td>
<td>Low/20K</td>
<td>Low</td>
<td>Low/20K</td>
<td>Low</td>
<td>Low/20K</td>
<td>Low</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>Enable</td>
<td>High</td>
<td>High</td>
<td>High</td>
<td>High</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Disable</td>
<td>Low/20K</td>
<td>Low</td>
<td>Low/20K</td>
<td>Low</td>
<td>Low/20K</td>
<td>Low</td>
</tr>
<tr>
<td>M1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Low/20K</td>
<td>Low</td>
<td>Running</td>
<td>Running</td>
<td>Low/20K</td>
<td>Low</td>
</tr>
</tbody>
</table>

### DOT Power Management Table

<table>
<thead>
<tr>
<th>PD#</th>
<th>CPU_STOP#</th>
<th>PCI_STOP#</th>
<th>PEREQ#</th>
<th>SMBus Register OE</th>
<th>DOT</th>
<th>DOT#</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X</td>
<td>1</td>
<td>X</td>
<td>Enable</td>
<td>Running</td>
<td>Running</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Enable</td>
<td>Low/20K</td>
<td>Low</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>Enable</td>
<td>Running</td>
<td>Running</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Enable</td>
<td>Running</td>
<td>Running</td>
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<tr>
<td>M1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Low/20K</td>
<td>Low</td>
</tr>
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</table>

### Singled-Ended Power Management Table

<table>
<thead>
<tr>
<th>PD#</th>
<th>CPU_STOP#</th>
<th>PCI_STOP#</th>
<th>PEREQ#</th>
<th>SMBus Register OE</th>
<th>PCIF/PCI Free-Run</th>
<th>PCIF/PCI Stoppable</th>
<th>USB48</th>
<th>REF</th>
<th>27M</th>
<th>SE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X</td>
<td>1</td>
<td>X</td>
<td>Enable</td>
<td>Running</td>
<td>Running</td>
<td>Running</td>
<td>Running</td>
<td>Running</td>
<td>Running</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Enable</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>Enable</td>
<td>Low</td>
<td>Low</td>
<td>Running</td>
<td>Running</td>
<td>Running</td>
<td>Running</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Disable</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>M1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
</tr>
</tbody>
</table>
## Differential Clock Tolerances

<table>
<thead>
<tr>
<th></th>
<th>CPU</th>
<th>SRC</th>
<th>DOT96</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>PPM tolerance</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>ppm</td>
</tr>
<tr>
<td>Cycle to Cycle Jitter Spread</td>
<td>-0.50%</td>
<td>-0.50%</td>
<td>0</td>
<td>%</td>
</tr>
</tbody>
</table>

## Clock Periods - Differential Outputs with Spread Spectrum Disabled

<table>
<thead>
<tr>
<th>SSC OFF</th>
<th>Center Freq. MHz</th>
<th>-c2c jitter</th>
<th>+SSC</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>100.00</td>
<td>9.94900</td>
<td>10.05100</td>
<td>ns</td>
<td>1,2</td>
</tr>
<tr>
<td></td>
<td>133.33</td>
<td>7.49255</td>
<td>7.50075</td>
<td>ns</td>
<td>1,2</td>
</tr>
<tr>
<td></td>
<td>166.67</td>
<td>5.99400</td>
<td>6.00060</td>
<td>ns</td>
<td>1,2</td>
</tr>
<tr>
<td></td>
<td>200.00</td>
<td>4.99500</td>
<td>5.00050</td>
<td>ns</td>
<td>1,2</td>
</tr>
<tr>
<td></td>
<td>266.67</td>
<td>3.74962</td>
<td>3.75037</td>
<td>ns</td>
<td>1,2</td>
</tr>
<tr>
<td></td>
<td>333.33</td>
<td>2.99970</td>
<td>3.00300</td>
<td>ns</td>
<td>1,2</td>
</tr>
<tr>
<td></td>
<td>400.00</td>
<td>2.49975</td>
<td>2.50025</td>
<td>ns</td>
<td>1,2</td>
</tr>
<tr>
<td>SRC</td>
<td>100.00</td>
<td>9.87400</td>
<td>10.12600</td>
<td>ns</td>
<td>1,2</td>
</tr>
<tr>
<td>DOT96</td>
<td>96.00</td>
<td>10.16563</td>
<td>10.66771</td>
<td>ns</td>
<td>1,2</td>
</tr>
</tbody>
</table>

## Clock Periods - Differential Outputs with Spread Spectrum Enabled

<table>
<thead>
<tr>
<th>SSC ON</th>
<th>Center Freq. MHz</th>
<th>-c2c jitter</th>
<th>+SSC</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>99.75</td>
<td>9.94906</td>
<td>10.10107</td>
<td>ns</td>
<td>1,2</td>
</tr>
<tr>
<td></td>
<td>133.00</td>
<td>7.49300</td>
<td>7.58300</td>
<td>ns</td>
<td>1,2</td>
</tr>
<tr>
<td></td>
<td>166.25</td>
<td>5.94944</td>
<td>6.03064</td>
<td>ns</td>
<td>1,2</td>
</tr>
<tr>
<td></td>
<td>199.50</td>
<td>4.98535</td>
<td>5.07533</td>
<td>ns</td>
<td>1,2</td>
</tr>
<tr>
<td></td>
<td>266.00</td>
<td>3.79655</td>
<td>3.76915</td>
<td>ns</td>
<td>1,2</td>
</tr>
<tr>
<td></td>
<td>332.50</td>
<td>2.99722</td>
<td>3.01532</td>
<td>ns</td>
<td>1,2</td>
</tr>
<tr>
<td></td>
<td>399.00</td>
<td>2.49772</td>
<td>2.56277</td>
<td>ns</td>
<td>1,2</td>
</tr>
<tr>
<td>SRC</td>
<td>99.75</td>
<td>9.87406</td>
<td>10.17607</td>
<td>ns</td>
<td>1,2</td>
</tr>
</tbody>
</table>

1. Guaranteed by design and characterization, not 100% tested in production.
2. All Long Term Accuracy specifications are guaranteed with the assumption that the crystal input is tuned to exactly 14.31818MHz.

---

*IDT™/ICS™ Embedded 56-Pin Industrial Temperature Range CK505 Compatible Clock* 

1612—08/19/09
General SMBus serial interface information for the ICS9ERS3125

How to Write:
• Controller (host) sends a start bit.
• Controller (host) sends the write address D2\(^{[H]}\)
• ICS clock will acknowledge
• Controller (host) sends the beginning byte location = N
• ICS clock will acknowledge
• Controller (host) sends the data byte count = X
• ICS clock will acknowledge
• Controller (host) starts sending **Byte N through Byte N + X -1**
• ICS clock will acknowledge each byte **one at a time**
• Controller (host) sends a Stop bit

How to Read:
• Controller (host) will send start bit.
• Controller (host) sends the write address D2\(^{[H]}\)
• ICS clock will acknowledge
• Controller (host) sends the begining byte location = N
• ICS clock will acknowledge
• Controller (host) will send a separate start bit.
• Controller (host) sends the read address D3\(^{[H]}\)
• ICS clock will acknowledge
• ICS clock will send the data byte count = X
• ICS clock sends **Byte N + X -1**
• ICS clock sends **Byte 0 through byte X (if X\(^{[H]}\) was written to byte 8)**.
• Controller (host) will need to acknowledge each byte
• Controller (host) will send a not acknowledge bit
• Controller (host) will send a stop bit

---

### Index Block Write Operation

<table>
<thead>
<tr>
<th>Controller (Host)</th>
<th>ICS (Slave/Receiver)</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>start bit</td>
</tr>
<tr>
<td>Slave Address D2(^{[H]})</td>
<td></td>
</tr>
<tr>
<td>WR</td>
<td>WRITE</td>
</tr>
<tr>
<td>Beginning Byte = N</td>
<td>ACK</td>
</tr>
<tr>
<td>Data Byte Count = X</td>
<td>ACK</td>
</tr>
<tr>
<td>ACK</td>
<td>X Byte</td>
</tr>
<tr>
<td>Beginning Byte N</td>
<td>ACK</td>
</tr>
<tr>
<td>0</td>
<td>ACK</td>
</tr>
<tr>
<td>0</td>
<td>ACK</td>
</tr>
<tr>
<td>0</td>
<td>ACK</td>
</tr>
<tr>
<td>Byte N + X - 1</td>
<td>ACK</td>
</tr>
<tr>
<td>P</td>
<td>stop bit</td>
</tr>
</tbody>
</table>

### Index Block Read Operation

<table>
<thead>
<tr>
<th>Controller (Host)</th>
<th>ICS (Slave/Receiver)</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>start bit</td>
</tr>
<tr>
<td>Slave Address D2(^{[H]})</td>
<td></td>
</tr>
<tr>
<td>WR</td>
<td>WRITE</td>
</tr>
<tr>
<td>Beginning Byte = N</td>
<td>ACK</td>
</tr>
<tr>
<td>Data Byte Count = X</td>
<td>ACK</td>
</tr>
<tr>
<td>ACK</td>
<td>X Byte</td>
</tr>
<tr>
<td>ACK</td>
<td>Beginning Byte N</td>
</tr>
<tr>
<td>0</td>
<td>ACK</td>
</tr>
<tr>
<td>0</td>
<td>ACK</td>
</tr>
<tr>
<td>0</td>
<td>ACK</td>
</tr>
<tr>
<td>Byte N + X - 1</td>
<td>ACK</td>
</tr>
<tr>
<td>N</td>
<td>Not acknowledge</td>
</tr>
<tr>
<td>P</td>
<td>stop bit</td>
</tr>
</tbody>
</table>
### Byte 0: FS Readback & PLL Selection Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>FSLC</td>
<td>CPU Freq. Sel. Bit (Most Significant)</td>
<td>R</td>
<td>See Table 1: CPU Frequency Select Table</td>
<td>Latch</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>FSLB</td>
<td>CPU Freq. Sel. Bit</td>
<td>R</td>
<td></td>
<td>Latch</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>FSLA</td>
<td>CPU Freq. Sel. Bit (Least Significant)</td>
<td>R</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>iAMT_EN</td>
<td>Set via SMBus or dynamically by CK505 if detects dynamic M1</td>
<td>R</td>
<td>Legacy Mode</td>
<td>iAMT Enabled</td>
<td>iAMT power on status</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>SRC_Main_SEL</td>
<td>Select source for SRC Main</td>
<td>RW</td>
<td>SRC Main = PLL5</td>
<td>SRC Main = PLL2</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>SATA_SEL</td>
<td>Select source for SATA clock</td>
<td>RW</td>
<td>SATA = SRC_Main</td>
<td>SATA = PLL3</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>PD_Restore</td>
<td>1 = on Power Down de-assert return to last known state 0 = clear all SMBus configurations as if cold power-on and go to latches open state This bit is ignored and treated at “1” if device is in iAMT mode.</td>
<td>RW</td>
<td>Configuration Not Saved</td>
<td>Configuration Saved</td>
<td>1</td>
</tr>
</tbody>
</table>

### Byte 1: DOT96 Select & PLL3 Quick Config Register,

**Note 1:** When 27.Select pin = 0, B1b7 Default = 1; When 27.Select pin = 1, Default = 0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>SRC0_SEL</td>
<td>Select SRC0 or DOT96</td>
<td>RW</td>
<td>SRC0</td>
<td>DOTS6</td>
<td>Note 1</td>
</tr>
<tr>
<td>6</td>
<td>PLL3_SSC_SEL</td>
<td>Select 0.5% down or center SSC</td>
<td>RW</td>
<td>Down spread</td>
<td>Center spread</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>PLL2_SSC_SEL</td>
<td>Select 0.5% center or down SSC</td>
<td>RW</td>
<td>Down</td>
<td>Center</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>PLL11_CF3</td>
<td>PLL11 Quick Config Bit 3</td>
<td>RW</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>PLL11_CF2</td>
<td>PLL11 Quick Config Bit 2</td>
<td>RW</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>PLL11_CF1</td>
<td>PLL11 Quick Config Bit 1</td>
<td>RW</td>
<td>Only applies if Byte 0, bit 2 = 0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>PLL1_CF0</td>
<td>PLL1 Quick Config Bit 0</td>
<td>RW</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>PCI_SEL</td>
<td>PCI_SEL</td>
<td>RW</td>
<td>PCI from PLL5</td>
<td>PCI from SRC_MAIN</td>
<td>1</td>
</tr>
</tbody>
</table>

### Byte 2: Single Ended Output Enable Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>REF_OE</td>
<td>Output enable for USB</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>USB_OE</td>
<td>Output enable for USB</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>PCI5_OE</td>
<td>Output enable for PCI5</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>PCI4_OE</td>
<td>Output enable for PCI4</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>PCI3_OE</td>
<td>Output enable for PCI3</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>PCI2_OE</td>
<td>Output enable for PCI2</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>PCI1_OE</td>
<td>Output enable for PCI1</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>PCI0_OE</td>
<td>Output enable for PCI0</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
</tbody>
</table>

### Byte 3: SRC Output Enable Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>SRC11_OE</td>
<td>Output enable for SRC11</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>SRC8/ITP_OE</td>
<td>Output enable for SRC8 or ITP</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>SRC7_OE</td>
<td>Output enable for SRC7</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>SRC6_OE</td>
<td>Output enable for SRC6</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>SRC4_OE</td>
<td>Output enable for SRC4</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
</tbody>
</table>

### Byte 4: SRC/CPU/DOT Output Enable & Spread Spectrum Disable Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>SRC3_OE</td>
<td>Output enable for SRC3</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>SATA/SRC2_OE</td>
<td>Output enable for SATA/SRC2</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>SRC1_OE</td>
<td>Output enable for SRC1</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>SRC9/DOT96_OE</td>
<td>Output enable for SRC9/DOT96</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>CPU1_OE</td>
<td>Output enable for CPU1</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>CPU0_OE</td>
<td>Output enable for CPU0</td>
<td>RW</td>
<td>Output Disabled</td>
<td>Output Enabled</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>PLL1/SCC_ON</td>
<td>Enable PLL1's spread modulation</td>
<td>RW</td>
<td>Spread Disabled</td>
<td>Spread Enabled</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>PLL2/SCC_ON</td>
<td>Enable PLL2's spread modulation</td>
<td>RW</td>
<td>Spread Disabled</td>
<td>Spread Enabled</td>
<td>1</td>
</tr>
</tbody>
</table>
### Byte 5 Clock Request Enable/Configuration Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>CR#_A_EN</td>
<td>Enable CR#_A (clk req) for SRC0 or SRC2</td>
<td>RW</td>
<td>Disable CR#_A</td>
<td>Enable CR#_A</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>CR#_A_SEL</td>
<td>Sets CR#_A to control either SRC0 or SRC2</td>
<td>RW</td>
<td>CR#_A -&gt; SRC0</td>
<td>CR#_A -&gt; SRC2</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>CR#_B_EN</td>
<td>Enable CR#_B (clk req) for SRC1 or SRC4</td>
<td>RW</td>
<td>Disable CR#_B</td>
<td>Enable CR#_B</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>CR#_B_SEL</td>
<td>Sets CR#_B to control either SRC1 or SRC4</td>
<td>RW</td>
<td>CR#_B -&gt; SRC1</td>
<td>CR#_B -&gt; SRC4</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>CR#_C_EN</td>
<td>Enable CR#_C (clk req) for SRC0 or SRC2</td>
<td>RW</td>
<td>Disable CR#_C</td>
<td>Enable CR#_C</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>CR#_C_SEL</td>
<td>Sets CR#_C to control either SRC0 or SRC2</td>
<td>RW</td>
<td>CR#_C -&gt; SRC0</td>
<td>CR#_C -&gt; SRC2</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>CR#_D_EN</td>
<td>Enable CR#_D (clk req) for SRC1 or SRC4</td>
<td>RW</td>
<td>Disable CR#_D</td>
<td>Enable CR#_D</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>CR#_D_SEL</td>
<td>Sets CR#_D to control either SRC1 or SRC4</td>
<td>RW</td>
<td>CR#_D -&gt; SRC1</td>
<td>CR#_D -&gt; SRC4</td>
<td>0</td>
</tr>
</tbody>
</table>

### Byte 6 Clock Request Enable/Configuration Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>CR#_E_EN</td>
<td>Enable CR#_E (clk req) for SRC6</td>
<td>RW</td>
<td>Disable CR#_E</td>
<td>Enable CR#_E</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>CR#_F_EN</td>
<td>Enable CR#_F (clk req) for SRC8</td>
<td>RW</td>
<td>Disable CR#_F</td>
<td>Enable CR#_F</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>Reserved</td>
<td></td>
<td>R</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Reserved</td>
<td></td>
<td>R</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td></td>
<td>R</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
<td></td>
<td>R</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>LCD/SRC1_STP_CRTL</td>
<td>If set, LCD_SS/SRC1 stops with PCI_STOP#</td>
<td>RW</td>
<td>Free Running</td>
<td>Stops with PCI_STOP# assertion</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>SRC0_STP_CRTL</td>
<td>If set, SRC0 stop with PCI_STOP#</td>
<td>RW</td>
<td>Free Running</td>
<td>Stops with PCI_STOP# assertion</td>
<td>0</td>
</tr>
</tbody>
</table>

### Byte 7 Vendor ID/Revision ID Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Rev Code Bit 3</td>
<td></td>
<td>R</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Rev Code Bit 2</td>
<td></td>
<td>R</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Rev Code Bit 1</td>
<td></td>
<td>R</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Rev Code Bit 0</td>
<td></td>
<td>R</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Vendor ID bit 3</td>
<td></td>
<td>R</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Vendor ID bit 2</td>
<td></td>
<td>R</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Vendor ID bit 1</td>
<td></td>
<td>R</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Vendor ID bit 0</td>
<td></td>
<td>R</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

### Byte 8 Device ID & Output Enable Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>Default (MLF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Device_ID3</td>
<td>Table of Device identifier codes, used for differentiating between CK505 package options, etc.</td>
<td>R</td>
<td>See Device ID Table 4</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>Device_ID2</td>
<td></td>
<td>R</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>Device_ID1</td>
<td></td>
<td>R</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>Device_ID0</td>
<td></td>
<td>R</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td></td>
<td>R</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
<td></td>
<td>R</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>27MHz_nonSS/SE1_OE</td>
<td>Output enable for SE1</td>
<td>RW</td>
<td>Disabled</td>
<td>Enabled</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>27MHz_SS/SE2_OE</td>
<td>Output enable for SE2</td>
<td>RW</td>
<td>Disabled</td>
<td>Enabled</td>
<td>1</td>
</tr>
</tbody>
</table>

### Byte 9 Test and Output Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PCI5S_STOP EN</td>
<td>Allows control of PCI5S with assertion of PCI_STOP#</td>
<td>RW</td>
<td>Free running</td>
<td>Stops with PCI_STOP# assertion</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>TME_Readback</td>
<td>Trusted Mode Enable (TME) strap status</td>
<td>R</td>
<td>normal operation</td>
<td>no overclocking</td>
<td>TME latch</td>
</tr>
<tr>
<td>5</td>
<td>Reserved</td>
<td></td>
<td>R</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Test Mode Select</td>
<td>Allows test select, ignores REF/FSCTestSel</td>
<td>RW</td>
<td>Outputs HI-Z</td>
<td>Outputs = REF/N</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>Test Mode Entry</td>
<td>Allows entry into test mode, ignores FSB/TestMode</td>
<td>RW</td>
<td>Normal operation</td>
<td>Test mode</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>CPU IO_VOUT2</td>
<td>CPU IO Output Voltage Select (Most Significant Bit)</td>
<td>RW</td>
<td>See Table 3: V.IO Selection (Default is 0.8V)</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>CPU IO_VOUT1</td>
<td>CPU IO Output Voltage Select</td>
<td>RW</td>
<td>See Table 3: V.IO Selection (Default is 0.8V)</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>CPU IO_VOUT0</td>
<td>CPU IO Output Voltage Select (Least Significant Bit)</td>
<td>RW</td>
<td>See Table 3: V.IO Selection (Default is 0.8V)</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>
### Byte 10 Output Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>27_SEL Latch Readback</td>
<td>Readback of 27_Select latch</td>
<td>R</td>
<td></td>
<td></td>
<td>Dot96/ LCD_SS /SE</td>
</tr>
<tr>
<td>6</td>
<td>PCI4 STOP EN</td>
<td>Allows control of PCI4 with assertion of PCI_STOP#</td>
<td>RW</td>
<td>Free running</td>
<td>Stoppable</td>
<td>PCI_STOP# assertion</td>
</tr>
<tr>
<td>5</td>
<td>PCI3 STOP EN</td>
<td>Allows control of PCI3 with assertion of PCI_STOP#</td>
<td>RW</td>
<td>Free running</td>
<td>Stoppable</td>
<td>PCI_STOP# assertion</td>
</tr>
<tr>
<td>4</td>
<td>PCI2 STOP EN</td>
<td>Allows control of PCI2 with assertion of PCI_STOP#</td>
<td>RW</td>
<td>Free running</td>
<td>Stoppable</td>
<td>PCI_STOP# assertion</td>
</tr>
<tr>
<td>3</td>
<td>PCI1 STOP EN</td>
<td>Allows control of PCI1 with assertion of PCI_STOP#</td>
<td>RW</td>
<td>Free running</td>
<td>Stoppable</td>
<td>PCI_STOP# assertion</td>
</tr>
<tr>
<td>2</td>
<td>PCI0 STOP EN</td>
<td>Allows control of PCI0 with assertion of PCI_STOP#</td>
<td>RW</td>
<td>Free running</td>
<td>Stoppable</td>
<td>PCI_STOP# assertion</td>
</tr>
<tr>
<td>1</td>
<td>CPU1 Stop Enable</td>
<td>Enables control of CPU1 with CPU_STOP#</td>
<td>RW</td>
<td>Free Running</td>
<td>Stoppable</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>CPU0 Stop Enable</td>
<td>Enables control of CPU0 with CPU_STOP#</td>
<td>RW</td>
<td>Free Running</td>
<td>Stoppable</td>
<td>1</td>
</tr>
</tbody>
</table>

### Byte 11 iAMT/CPU2 Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Reserved</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Reserved</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Reserved</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>CPU2_AMT_EN</td>
<td>M1 mode clk enable, only if ITP_EN=1</td>
<td>RW</td>
<td>Disable</td>
<td>Enable</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>CPU1_AMT_EN</td>
<td>M1 mode clk enable</td>
<td>RW</td>
<td>Disable</td>
<td>Enable</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>Reserved</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>CPU2 Stop Enable</td>
<td>Enables control of CPU2 with CPU_STOP#</td>
<td>RW</td>
<td>Free Running</td>
<td>Stoppable</td>
<td>1</td>
</tr>
</tbody>
</table>

### Byte 12 Byte Count Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Reserved</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>BC5</td>
<td>Read Back byte count register, max bytes = 32</td>
<td>RW</td>
<td>-</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>BC4</td>
<td>-</td>
<td>RW</td>
<td>-</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>BC3</td>
<td>-</td>
<td>RW</td>
<td>-</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>BC2</td>
<td>-</td>
<td>RW</td>
<td>-</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>BC1</td>
<td>-</td>
<td>RW</td>
<td>-</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>BC0</td>
<td>-</td>
<td>RW</td>
<td>-</td>
<td>-</td>
<td>1</td>
</tr>
</tbody>
</table>

### Byte 13 Single Ended Output Slew Rate Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
<th>Type</th>
<th>0</th>
<th>1</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>REF</td>
<td>Slew Rate Control</td>
<td>RW</td>
<td>00 = Hi-Z</td>
<td>01 = 1.4 V/ns</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>REF</td>
<td>Slew Rate Control</td>
<td>RW</td>
<td>10 = 2.0 V/ns</td>
<td>11 = 2.4 V/ns</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>27M_FIX</td>
<td>Slew Rate Control</td>
<td>RW</td>
<td>00 = Hi-Z</td>
<td>01 = 1.4 V/ns</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>27M_FIX</td>
<td>Slew Rate Control</td>
<td>RW</td>
<td>10 = 2.0 V/ns</td>
<td>11 = 2.4 V/ns</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>27M_SS</td>
<td>Slew Rate Control</td>
<td>RW</td>
<td>00 = Hi-Z</td>
<td>01 = 1.4 V/ns</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>27M_SS</td>
<td>Slew Rate Control</td>
<td>RW</td>
<td>10 = 2.0 V/ns</td>
<td>11 = 2.4 V/ns</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>Reserved</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Reserved</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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### Byte 14 Reserved

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**Byte 17 SRC Output Control Register**

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<tbody>
<tr>
<td>7</td>
<td>S2A/SRC2 STP CRTL If set, S2A/SRC2 stops with PCI_STOP#</td>
<td>RW Free Running</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>SRC3 STP CRTL If set, SRC3 stops with PCI_STOP#</td>
<td>RW Free Running</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>5</td>
<td>SRC4 STP CRTL If set, SRC4 stops with PCI_STOP#</td>
<td>RW Free Running</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>SRC6 STP CRTL If set, SRC6 stops with PCI_STOP#</td>
<td>RW Free Running</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>SRC7 STP CRTL If set, SRC7 stops with PCI_STOP#</td>
<td>RW Free Running</td>
<td></td>
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<td></td>
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<tr>
<td>2</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>1</td>
<td>SRC8 STP CRTL If set, SRC8 stops with PCI_STOP#</td>
<td>RW Free Running</td>
<td></td>
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<td></td>
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<tr>
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**Byte 18 Differential Output Control Register**

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<tr>
<td>6</td>
<td>SRC11 STP CRTL If set, SRC11 stops with PCI_STOP#</td>
<td>RW Free Running</td>
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<tr>
<td>5</td>
<td>SRC/CPUITP_SRC8 IO_VOUT2 SRC &amp; CPUITP_SRC8IO Output Voltage Select (Most Significant Bit)</td>
<td>RW</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>4</td>
<td>SRC/CPUITP_SRC8 IO_VOUT1 SRC IO &amp; CPUITP_SRC8IO Output Voltage Select</td>
<td>RW</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>SRC/CPUITP_SRC8 IO_VOUT0 SRC &amp; CPUITP_SRC8IO Output Voltage Select (Least Significant Bit)</td>
<td>RW</td>
<td></td>
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<tr>
<td>2</td>
<td>S2A/SRC2 IO_VOUT2 S2A SRC2 IO Output Voltage Select (Most Significant Bit)</td>
<td>RW See Table 3: V.IO Selection (Default is 0.8V)</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>1</td>
<td>S2A/SRC2 IO_VOUT1 S2A SRC2 IO Output Voltage Select</td>
<td>RW See Table 3: V.IO Selection (Default is 0.8V)</td>
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<tr>
<td>0</td>
<td>S2A/SRC2 IO_VOUT0 S2A SRC2 IO Output Voltage Select (Least Significant Bit)</td>
<td>RW</td>
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### Byte 19 Differential Output Control Register

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<tbody>
<tr>
<td>7</td>
<td>LCD_SS (SRC1) IO_VOUT2</td>
<td>LCD_SS IO Output Voltage Select (Most Significant Bit)</td>
<td>RW</td>
<td>See Table 3: V_IO Selection (Default is 0.8V)</td>
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<td>6</td>
<td>LCD_SS (SRC1) IO_VOUT1</td>
<td>LCD_SS IO Output Voltage Select</td>
<td>RW</td>
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<td></td>
<td>0</td>
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<tr>
<td>5</td>
<td>LCD_SS (SRC1) IO_VOUT0</td>
<td>LCD_SS IO Output Voltage Select (Least Significant Bit)</td>
<td>RW</td>
<td></td>
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</tr>
<tr>
<td>4</td>
<td>SRC0/DOT96 IO_VOUT2</td>
<td>SRC0_DOT96 IO Output Voltage Select (Most Significant Bit)</td>
<td>RW</td>
<td>See Table 3: V_IO Selection (Default is 0.8V)</td>
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<tr>
<td>3</td>
<td>SRC0/DOT96 IO_VOUT1</td>
<td>SRC0_DOT96 IO Output Voltage Select</td>
<td>RW</td>
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<td>0</td>
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<tr>
<td>2</td>
<td>SRC0/DOT96 IO_VOUT0</td>
<td>SRC0_DOT96 IO Output Voltage Select (Least Significant Bit)</td>
<td>RW</td>
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### Byte 20 Single Ended Slew Rate Control Register

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<td>RW</td>
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<td>48MHz</td>
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<td>PCI5</td>
<td>Slew Rate Control</td>
<td>RW</td>
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<tr>
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<td>RW</td>
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<td>3</td>
<td>PCI4</td>
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### Byte 21 Single Ended Slew Rate & MN Enable Control Register

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<td>Slew Rate Control</td>
<td>RW</td>
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<td>PCI1</td>
<td>Slew Rate Control</td>
<td>RW</td>
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<td>RW</td>
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## Test Clarification Table

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<th>Comments</th>
<th>HW Pin</th>
<th>SW Pin</th>
<th>TEST ENTRY BIT</th>
<th>REF/N or HI-Z</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CK_PWRG=1 w/ TEST_SEL = 1 to enter test mode</td>
<td>&lt;2.0V: X 0 0</td>
<td>NORMAL</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Cycle power to disable test mode</td>
<td>&gt;2.0V: 0 X 0</td>
<td>HI-Z</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FS LC/TEST_SEL --&gt;3-level latched input</td>
<td>&gt;2.0V: 0 X 1</td>
<td>REF/N</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>If CK_PWRG=1 w/ V&gt;2.0V then use TEST_SEL</td>
<td>&gt;2.0V: 1 X 1</td>
<td>REF/N</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>If CK_PWRG=1 w/ V&lt;2.0V then use FS LC</td>
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<td></td>
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<tr>
<td>FSLB/TEST_MODE --&gt; low Vth input</td>
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<tr>
<td>TEST_MODE is a real time input</td>
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<tr>
<td>If TEST_SEL HW pin is 0 after CK_PWRG=1,</td>
<td>&lt;2.0V: X 1 0</td>
<td>HI-Z</td>
<td></td>
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</tr>
<tr>
<td>test mode can be invoked through B9b3.</td>
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<tr>
<td>If test mode is invoked by B9b3, only B9b4 is used to select HI-Z or REF/N</td>
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<tr>
<td>FSLB/TEST_MODE pin is not used.</td>
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<tr>
<td>Cycle power to disable test mode, one shot control</td>
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</table>

B9b3: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)
B9b4: 1= REF/N, Default = 0 (HI-Z)
THERMALLY ENHANCED, VERY THIN, FINE PITCH
QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIONS

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<th>MAX.</th>
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<tr>
<td>Nd</td>
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<tr>
<td>Ne</td>
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DIMENSIONS (mm)

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<th>MAX.</th>
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<td>e</td>
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<tr>
<td>D x E</td>
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<td>8.00</td>
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<tr>
<td>D2 MIN.</td>
<td>4.35</td>
<td>4.65</td>
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<tr>
<td>D2 MAX.</td>
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<tr>
<td>E2 MIN.</td>
<td>5.05</td>
<td>5.35</td>
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<tr>
<td>E2 MAX.</td>
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<td>0.5</td>
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Ordering Information

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<th>Shipping Packaging</th>
<th>Package</th>
<th>Temperature</th>
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<tr>
<td>9ERS3125BKILF</td>
<td>Tubes</td>
<td>56-pin MLF</td>
<td>-40 to +85°C</td>
</tr>
<tr>
<td>9ERS3125BKILFT</td>
<td>Tape and Reel</td>
<td>56-pin MLF</td>
<td>-40 to +85°C</td>
</tr>
</tbody>
</table>

Parts that are ordered with a “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant. Due to package size constraints, actual top-side marking may differ from the full orderable part number.
Embedded 56-Pin Industrial Temperature Range CK505 Compatible Clock Datasheet

Revision History

<table>
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<th>Description</th>
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<td>Initial Release</td>
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<tr>
<td>A</td>
<td>08/19/09</td>
<td>Released to final</td>
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</tbody>
</table>

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