**Si5347/46, Si5345/44/42, Si5341/40**

**Silicon Revision A1 Errata**

### Errata Status Summary

<table>
<thead>
<tr>
<th>Errata #</th>
<th>Title</th>
<th>Impact</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Output frequency limited to 710 MHz.</td>
<td>Major</td>
<td>May be fixed in a future revision.</td>
</tr>
<tr>
<td>2</td>
<td>OSC startup issue w/ XTALs if Tj &gt; 110 °C.</td>
<td>Major</td>
<td>Fixed in silicon revision B.</td>
</tr>
<tr>
<td>3</td>
<td>Input-to-Output delay is not consistent.</td>
<td>Major</td>
<td>No workaround. Will be fixed in a future revision.</td>
</tr>
<tr>
<td>4</td>
<td>Output-to-Output skew is not consistent.</td>
<td>Major</td>
<td>No workaround. Will be fixed in a future revision.</td>
</tr>
<tr>
<td>5</td>
<td>LVCMOS Hi-Z mode impedance too low.</td>
<td>Major</td>
<td>No workaround. Will be fixed in a future revision.</td>
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<tr>
<td>6</td>
<td>LOS and OOF sticky status bits cannot be cleared.</td>
<td>Minor</td>
<td>No workaround. Will be fixed in a future revision.</td>
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</table>

Impact definition: Each erratum is marked with an impact, as defined below:
- **Minor** – Workaround exists.
- **Major** – Errata that do not conform to the data sheet or standard.
- **Information** – The device behavior is not ideal but acceptable. Typically, the data sheet will be changed to match the device behavior.
- This document applies to Ordering Part Numbers (OPNs) which refer to product Revision A (silicon revision A1). For example: Si5345A-A-GM or Si5341A-Axxxxx-GM, where xxxxx is the custom OPN ID.
- Silicon revision B will have OPNs with B in the product revision. For example: Si5345A-B-GM or Si5341A-Bxxxxx-GM, where xxxxx is the custom OPN ID.
Errata Details

1. **Description:**
The VCO operating frequency range limits the maximum generated clock output frequency.

**Impact:**
Frequencies can be generated up to 710 MHz and not 800 MHz as stated in the data sheet. ClockBuilder Pro currently limits output frequencies to 710 MHz.

**Workaround:**
There is no workaround for this issue at this time.

**Resolution:**
This limitation may be fixed in a future revision.

**Description:**
The oscillator circuit (OSC) may not start up when running the chip at high temperatures. The ESD protection circuit on XA/XB interacts with an internal regulator for the OSC circuit at start up. The problem occurs when the junction temperature is above 110 °C.

**Impact:**
If the chip is powered-up, or a hard or soft reset is performed at high temperatures, the DSPLL will not be able to achieve lock and output clocks will not be generated.

**Workaround:**
There is no workaround for this issue. Refer to ClockBuilder Pro’s power dissipation report to help determine your design’s effective junction temperature.

**Resolution:**
This issue is fixed in silicon revision B.

2. **Description:**
The input-to-output delay is not consistent when running the chip at high temperatures. The problem occurs when the junction temperature is above 110 °C.

**Impact:**
If the chip is powered-up, or a hard or soft reset is performed at high temperatures, the input-to-output delay may exceed the data sheet specification.

**Workaround:**
There is no workaround for this issue.

**Resolution:**
This erratum will be fixed in a future revision.
3. **Description:**
The output-to-output delay is not consistent when running the chip at high temperatures. The problem occurs when the junction temperature is above 110 °C.

**Impact:**
If the chip is powered-up, or a hard or soft reset is performed at high temperatures, the output-to-output delay may exceed the data sheet specification of 100 ps.

**Workaround:**
There is no workaround for this issue.

**Resolution:**
This erratum will be fixed in a future revision.

4. **Description:**
An LVCMOS output can be configured to disable in a low logic state, a high logic state, or in high-impedance mode. The disable in high-impedance state does not meet the data sheet specification.

**Impact:**
The LVCMOS high-impedance mode should not be used.

**Workaround:**
Select the disable state as stop-high or stop-low.

**Resolution:**
This erratum will be fixed in a future revision.

5. **Description:**
LOS and OOF sticky status bits cannot be cleared unless its fault monitor is disabled.

**Impact:**
LOS and OOF sticky (flag) bits will always remain set whenever asserted. Clearing the sticky bit(s) will have no effect.

**Workaround:**
It is possible to clear a sticky bit by temporarily disabling its fault monitor. Once disabled, the bit can be cleared and the fault monitor re-enabled.

**Resolution:**
This erratum will be fixed in a future revision.