BLC10G27LS-320AVT

Power LDMOS transistor

Rev. 2 — 1 December 2017

AMPLEON

Product data sheet

1. Product profile

1.1 General description

320 W LDMOS packaged asymmetrical Doherty power transistor for base station applications at frequencies from 2500 MHz to 2700 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in the Doherty demo board.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	2500 to 2700	28	50	16	45	−30 [1]

[1] Test signal: 3GPP test model 1; 1 to 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

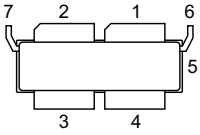
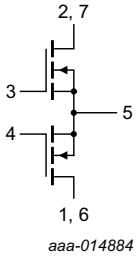
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Decoupling leads to enable improved video bandwidth
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifier for W-CDMA base stations and multi carrier applications in the 2500 MHz to 2700 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		
2	drain1 (main)		
3	gate1 (main)		
4	gate2 (peak)		
5	source [1]		
6	video decoupling (peak)		
7	video decoupling (main)		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC10G27LS-320AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1258-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		−6	+13	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 80 W	0.24	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 100 mA	1.5	2	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 400 mA	1.7	2.2	2.7	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 2.37 V; V_{DS} = 10 V	-	20	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 5.0 A	-	12	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 2.37 V; I_D = 3.5 A	-	125	170	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.08 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 208 mA	1.5	2	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 1000 mA	1.7	2.2	2.7	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 2.37 V; V_{DS} = 10 V	-	39	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 10.4 A	-	23	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 2.37 V; I_D = 7.28 A	-	63.0	96.6	mΩ

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; RF performance at V_{DS} = 28 V; I_{Dq} = 400 mA (main); $V_{GS(amp)peak}$ = 1 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 2496 MHz to 2690 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 50 W	14.6	15.4	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 50 W	-	−10	−6	dB
η_D	drain efficiency	$P_{L(AV)}$ = 50 W	37.6	42	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 50 W	-	−32	−27	dBc

7. Test information

7.1 Ruggedness in Doherty operation

The BLC10G27LS-320AVT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 400 mA (main); $V_{GS(amp)peak}$ = 1 V; P_L = 200 W (CW); f = 2496 MHz.

7.2 Impedance information

Table 8. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 600 mA; V_{DS} = 28 V. Typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
2500	1.8 – j5.6	2.1 – j4.1	140	61.0	17.1
2600	2.9 – j6.2	2.0 – j3.8	140	61.5	17.0
2700	5.4 – j6.0	1.8 – j4.2	140	57.0	16.6
Maximum drain efficiency load					
2500	1.8 – j5.6	3.1 – j3.0	111	65.2	18.6
2600	2.9 – j6.2	3.1 – j3.0	107	65.8	18.7
2700	5.4 – j6.0	2.4 – j3.2	119	63.7	18.1

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

Table 9. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 1200 mA; V_{DS} = 28 V. Typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
2500	2.2 – j6.4	2.4 – j3.9	270	59.1	16.5
2600	4.6 – j7.3	2.4 – j3.9	266	56.9	15.9
2700	10.7 – j5.0	2.4 – j3.9	254	55.6	16.5
Maximum drain efficiency load					
2500	2.2 – j6.4	3.4 – j2.7	221	64.4	17.9
2600	4.6 – j7.3	2.8 – j2.7	227	62.0	17.1
2700	10.7 – j5.0	2.6 – j2.5	207	60.8	17.8

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

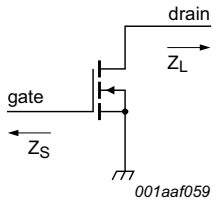
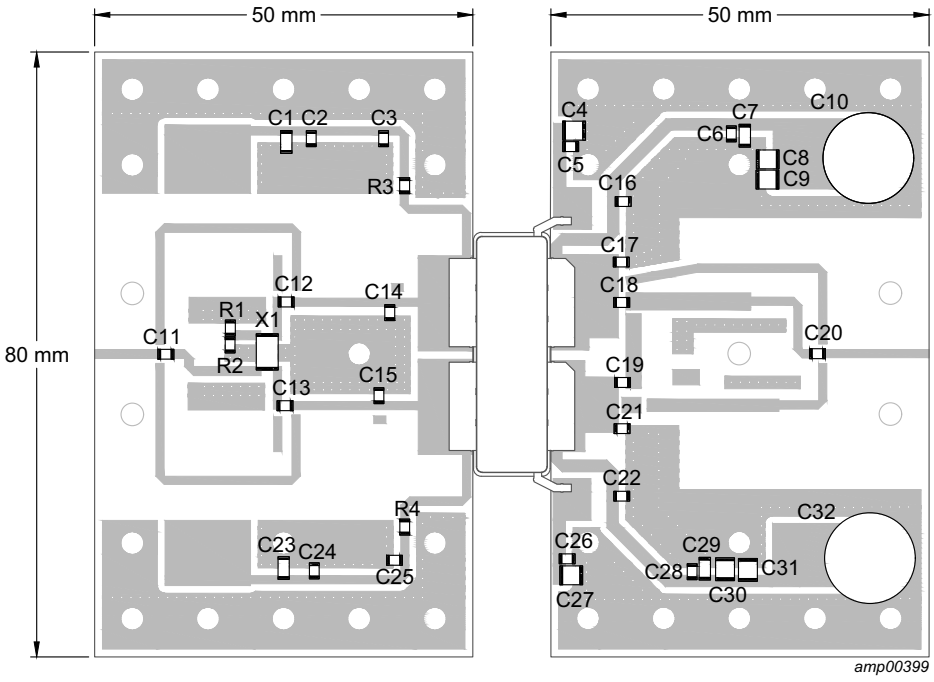


Fig 1. Definition of transistor impedance

7.3 VBW in Doherty operation

The BLC10G27LS-320AVT shows 120 MHz (typical) video bandwidth in Doherty test circuit in 2600 MHz band at V_{DS} = 28 V; I_{Dq} = 400 mA (main); $V_{GS(amp)peak}$ = 1 V;

7.4 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; thickness = 0.508 mm.

See Table 10 for a list of components.

Fig 2. Component layout for test circuit

Table 10. List of components

See Figure 2 for component layout.

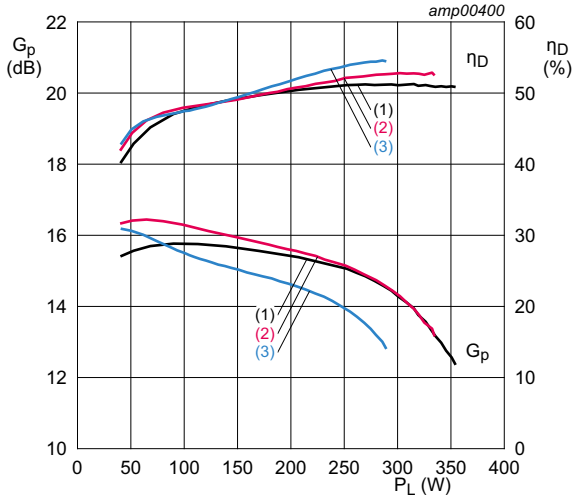
Component	Description	Value	Remarks
C1, C7, C23, C29	multilayer ceramic chip capacitor	1 μF	Murata
C2, C3, C5, C6, C11, C12, C13, C16, C18, C19, C20, C22, C24, C25, C26, C28	multilayer ceramic chip capacitor	20 pF	ATC 600F
C4, C8, C9, C27, C30, C31	multilayer ceramic chip capacitor	4.7 μF	Murata
C10, C32	electrolytic capacitor	2200 μF,63 V	
C14, C15	multilayer ceramic chip capacitor	0.7 pF	ATC 600F
C17	multilayer ceramic chip capacitor	0.2 pF	ATC 600F
C21	multilayer ceramic chip capacitor	1.3 pF	ATC 600F

Table 10. List of components *…continued*
See Figure 2 for component layout.

Component	Description	Value	Remarks
R1, R2	resistor	100 Ω	SMD 1206
R3, R4	resistor	5.1 Ω	SMD 0805
X1	coupler		Anaren: X3C25F1-02S

7.5 Graphical data

7.5.1 Pulsed CW



V_{DS} = 28 V; I_{Dq} = 400 mA; $V_{GS(amp)peak}$ = 1 V.

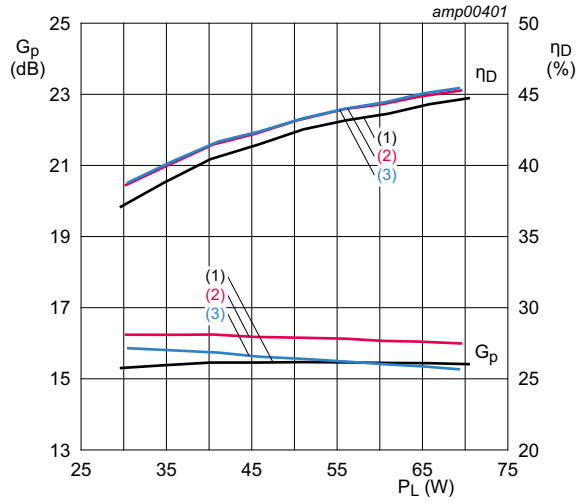
(1) f = 2496 MHz

(2) f = 2600 MHz

(3) f = 2690 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values

7.5.2 1-Carrier W-CDMA



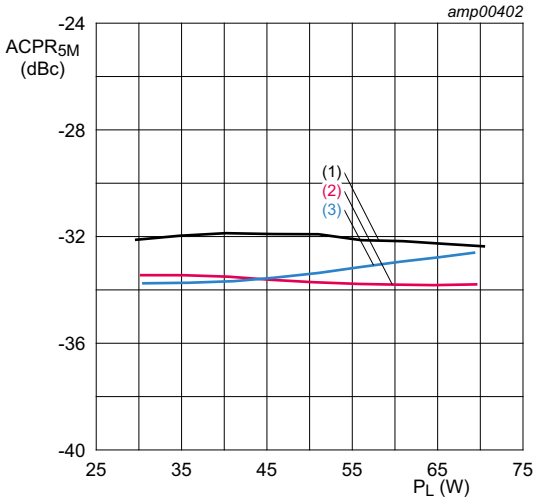
V_{DS} = 28 V; I_{Dq} = 400 mA; $V_{GS(amp)peak}$ = 1 V.

(1) f = 2496 MHz

(2) f = 2600 MHz

(3) f = 2690 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



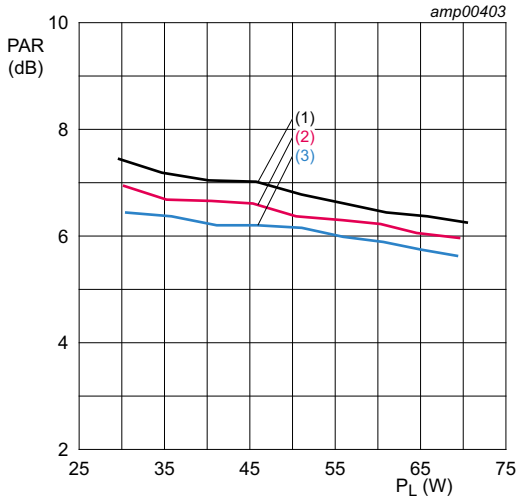
V_{DS} = 28 V; I_{Dq} = 400 mA; $V_{GS(amp)peak}$ = 1 V.

(1) f = 2496 MHz

(2) f = 2600 MHz

(3) f = 2690 MHz

Fig 5. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 400 mA; $V_{GS(amp)peak}$ = 1 V.

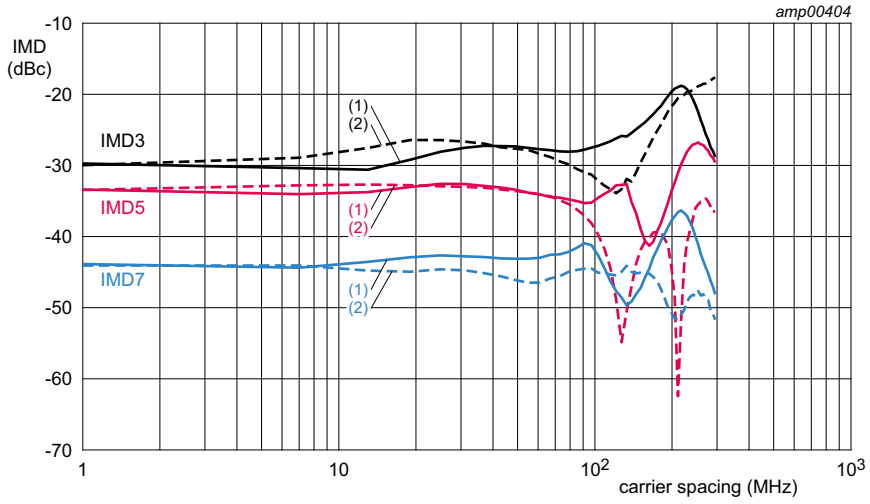
(1) f = 2496 MHz

(2) f = 2600 MHz

(3) f = 2690 MHz

Fig 6. Peak-to-average ratio as a function of output power; typical values

7.5.3 2-Tone VBW



V_{DS} = 28 V; I_{Dq} = 400 mA; $V_{GS(amp)peak}$ = 0.8 V; f_c = 2600 MHz.

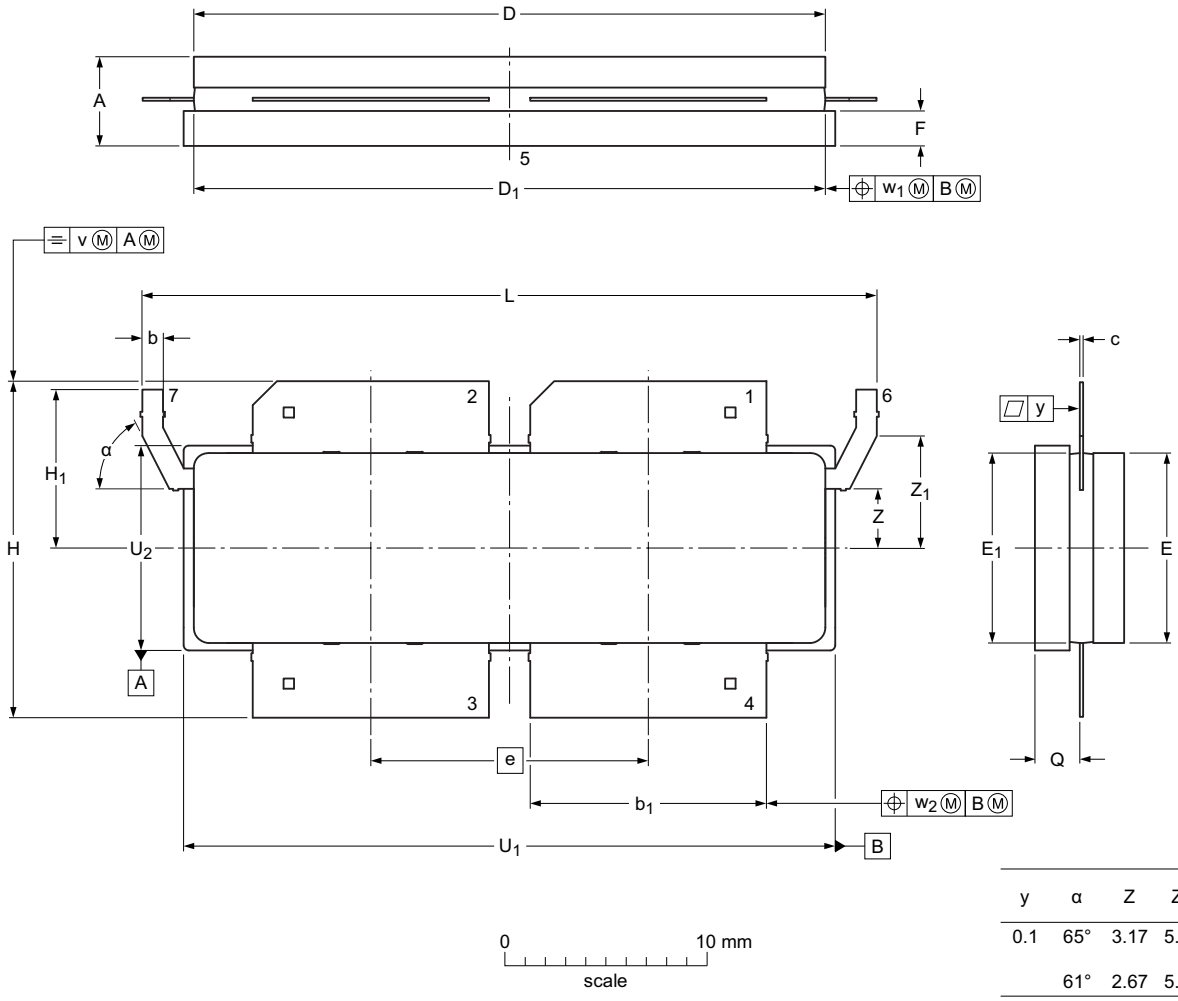
(1) IMD low

(2) IMD high

Fig 7. VBW capability in Doherty demo board

8. Package outline

Air cavity plastic earless flanged package; 6 leads **SOT1258-1**



y	α	Z	Z_1
0.1	65°	3.17	5.79
	61°	2.67	5.29

Dimensions

Unit		A	b	b_1	c	D	D_1	E	E_1	e	L	F	H	H_1	Q(1)	U_1	U_2	v	w_1	w_2
mm	max	4.65	1.12	11.78	0.2	31.44	31.34	9.60	9.50	13.72	36.42	1.83	16.71	8.12	2.33	32.33	10.23	0.5	0.5	0.5
	nom																			
	min	4.18	0.91	11.58	0.1	31.04	31.14	9.20	9.30		36.22	1.63	16.51	7.62	2.13	32.13	10.03			

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1258-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1258-1						~~14-02-24~~ 17-08-31

Fig 8. Package outline SOT1258-1

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC10G27LS-320AVT v.2	20171201	Product data sheet	-	BLC10G27LS-320AVT v.1
Modifications:	• Table 7 on page 3: value $P_{L(AV)}$ corrected			
BLC10G27LS-320AVT v.1	20171116	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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