

FCPF165N65S3R0L

Power MOSFET, N-Channel, SUPERFET[®] III, Easy Drive, 650 V, 19 A, 165 mΩ

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate. Consequently, SUPERFET III MOSFET Easy drive series helps manage EMI issues and allows for easier design implementation.

Features

- 700 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 140\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 35\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 345\text{ pF}$)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

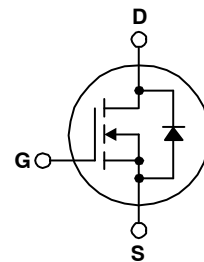
- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Industrial Power Supplies
- Lighting / Charger / Adapter



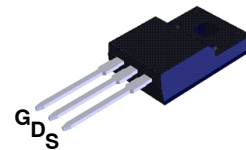
ON Semiconductor[®]

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V_{DS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	165 mΩ @ 10 V	19 A

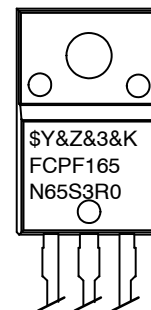


N-CHANNEL MOSFET



TO-220F-3LD
CASE 340BF

MARKING DIAGRAM



- \$Y = ON Semiconductor Logo
- &Z = Assembly Plant Code
- &3 = Data Code (Year & Week)
- &K = Lot
- FCPF165N65S3R0 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FCPF165N65S3R0L

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter	FCPF165N65S3R0L	Unit
V _{DSS}	Drain to Source Voltage	650	V
V _{GSS}	Gate to Source Voltage	- DC	±30
		- AC (f > 1 Hz)	±30
I _D	Drain Current:	- Continuous (T _C = 25°C)	19
		- Continuous (T _C = 100°C)	12.3
I _{DM}	Drain Current:	- Pulsed (Note 1)	47.5
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	87	mJ
I _{AS}	Avalanche Current (Note 2)	2.7	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	0.35	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	
P _D	Power Dissipation	(T _C = 25°C)	35
		Derate Above 25°C	0.28
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to + 150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 2.7 A, R_G = 25 Ω, starting T_J = 25 °C.
3. I_{SD} ≤ 9.5 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25 °C.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FCPF165N65S3R0L	FCPF165N65S3R0	TO-220F	Tube	N/A	N/A	50 Units

THERMAL CHARACTERISTICS

Symbol	Parameter	FCPF165N65S3R0L	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	3.56	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	62.5	

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650	–	–	V
BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C	–	0.64	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 520 V, T _C = 125 °C	–	1.39	–	
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 1.9 mA	2.5	–	4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 9.5 A	–	140	165	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 9.5 A	–	12	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz	–	1415	–	pF
C _{oss}	Output Capacitance		–	35	–	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	345	–	pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	48	–	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 400 V, I _D = 9.5 A, V _{GS} = 10 V (Note 4)	–	35	–	nC
Q _{gs}	Gate to Source Gate Charge		–	8.3	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	15	–	nC
ESR	Equivalent Series Resistance	F = 1 MHz	–	0.5	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 9.5 A, V _{GS} = 10 V, R _g = 4.7 Ω (Note 4)	–	17	–	ns
t _r	Turn-On Rise Time		–	16	–	ns
t _{d(off)}	Turn-Off Delay Time		–	43	–	ns
t _f	Turn-Off Fall Time		–	5	–	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current	–	–	19	A	
I _S	Maximum Pulsed Source to Drain Diode Forward Current	–	–	47.5	A	
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 9.5 A	–	–	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 9.5 A, di/dt = 100 A/μs	–	323	–	ns
Q _{rr}	Reverse Recovery Charge		–	5.2	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

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TYPICAL CHARACTERISTICS

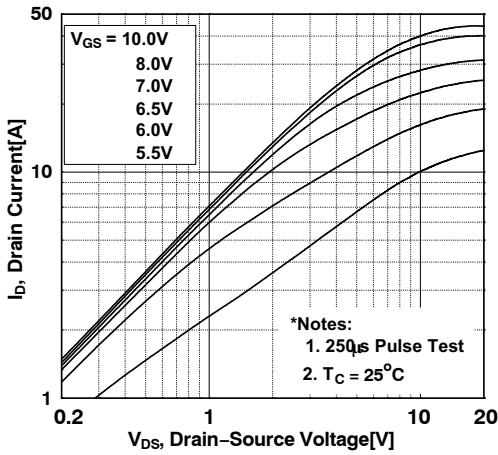


Figure 1. On-Region Characteristics

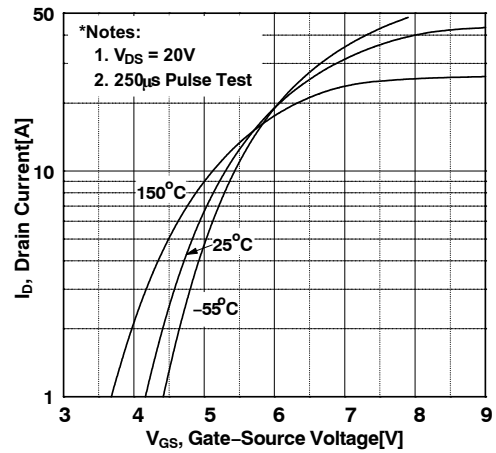


Figure 2. Transfer Characteristics

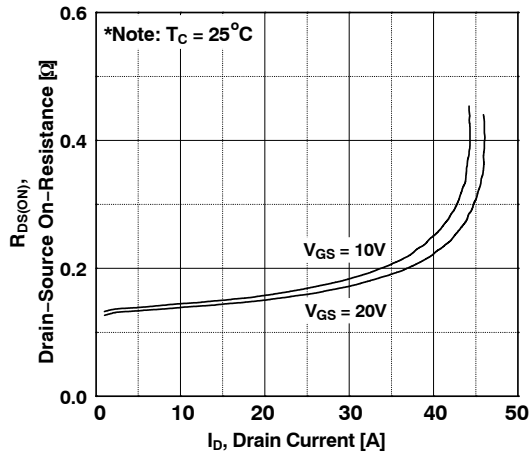


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

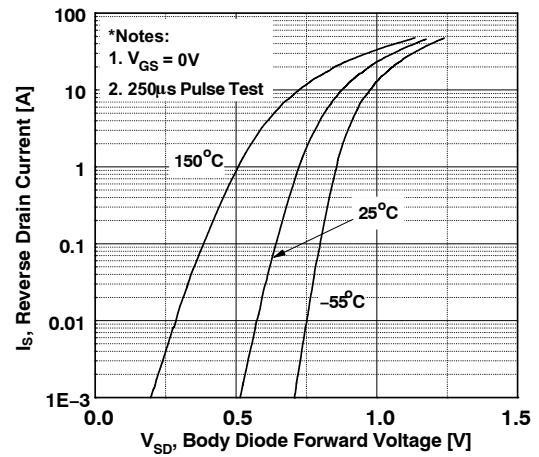


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

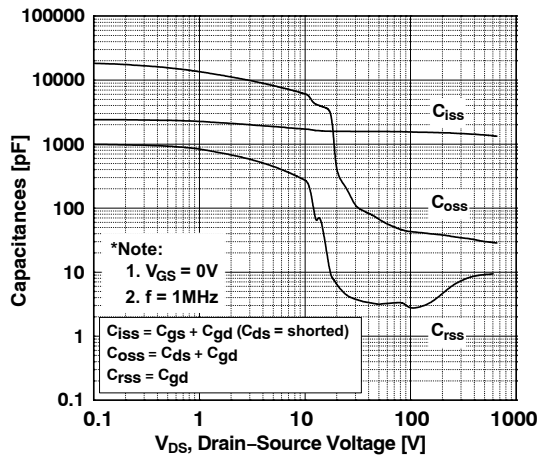


Figure 5. Capacitance Characteristics

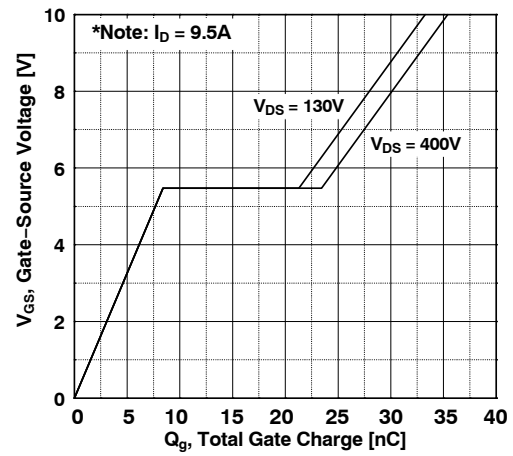


Figure 6. Gate Charge Characteristics

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TYPICAL CHARACTERISTICS

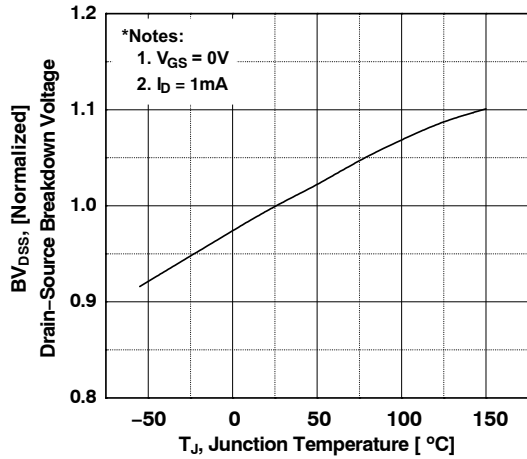


Figure 7. Breakdown Voltage Variation vs. Temperature

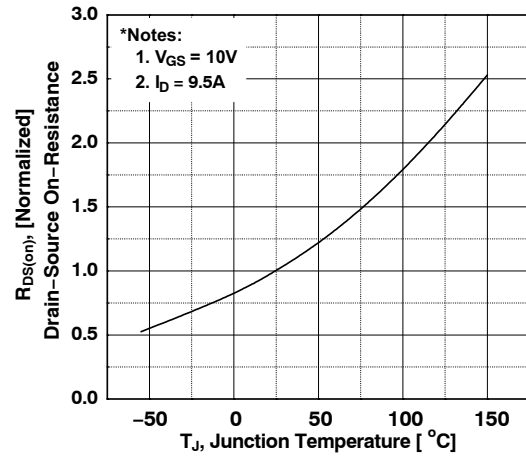


Figure 8. On-Resistance Variation vs. Temperature

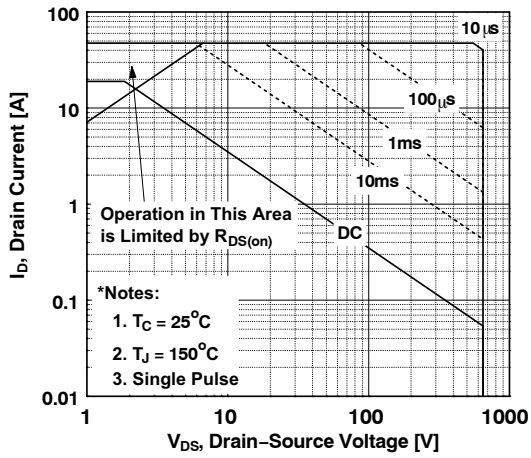


Figure 9. Maximum Safe Operating Area

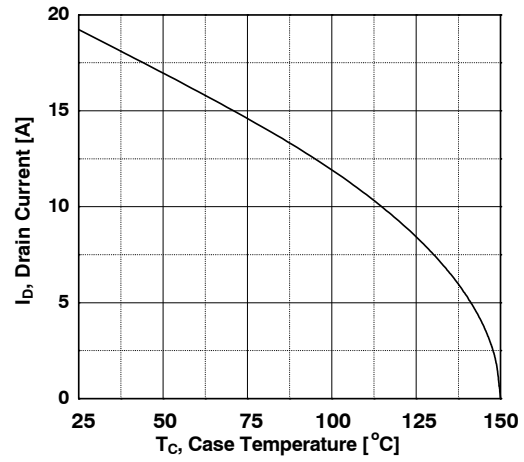


Figure 10. Maximum Drain Current vs. Case Temperature

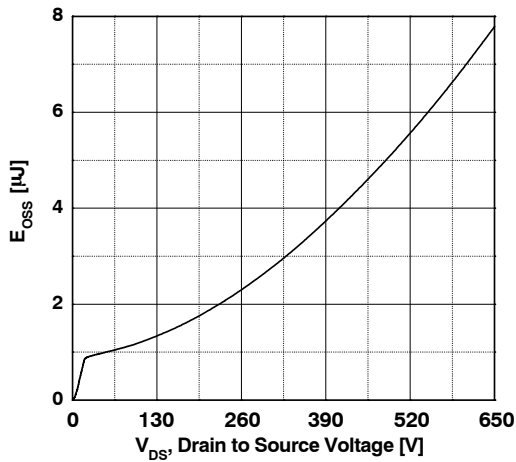


Figure 11. E_{oss} vs. Drain to Source Voltage

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TYPICAL CHARACTERISTICS

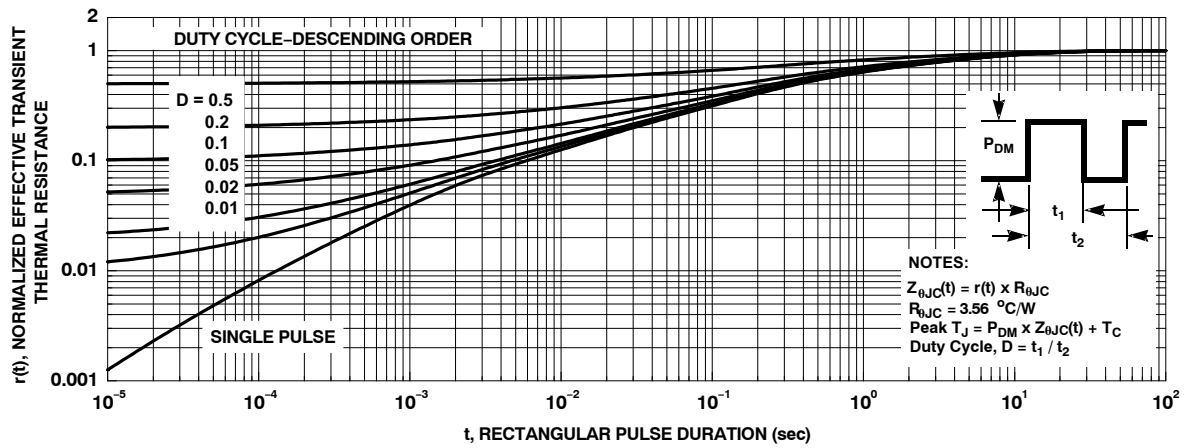


Figure 12. Transient Thermal Response Curve

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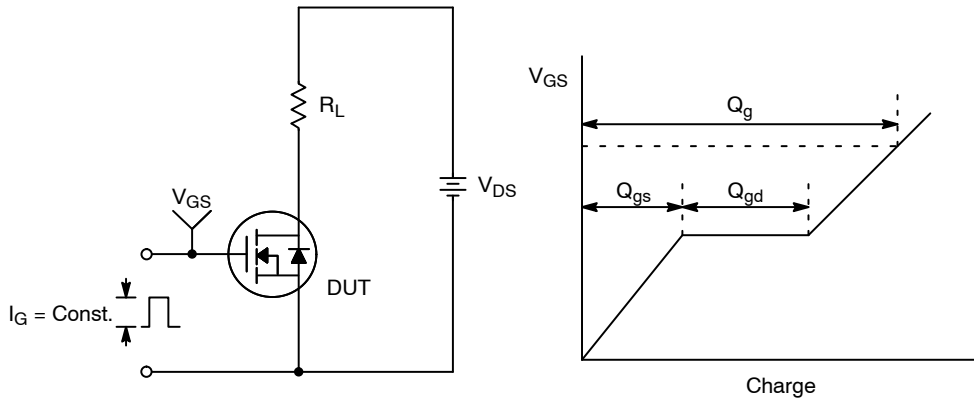


Figure 13. Gate Charge Test Circuit & Waveform

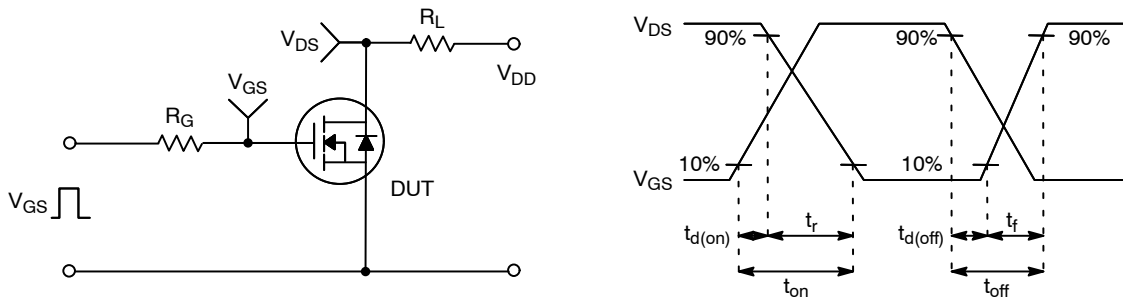


Figure 14. Resistive Switching Test Circuit & Waveforms

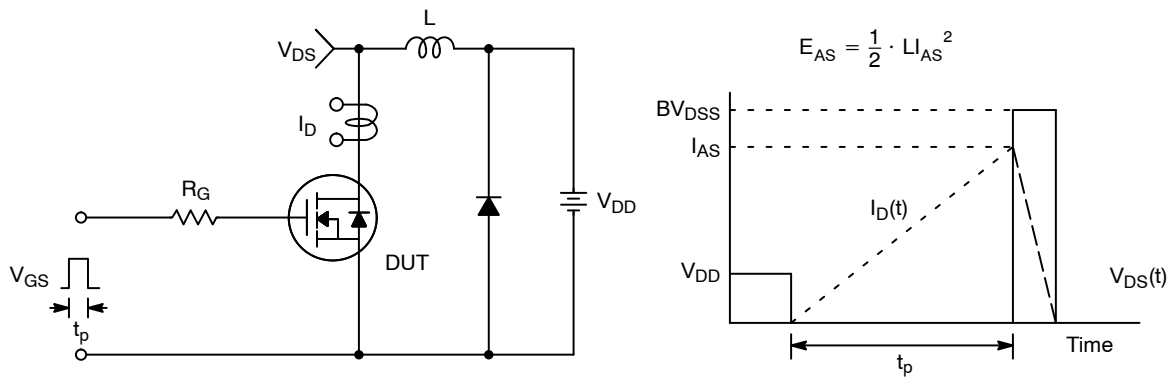


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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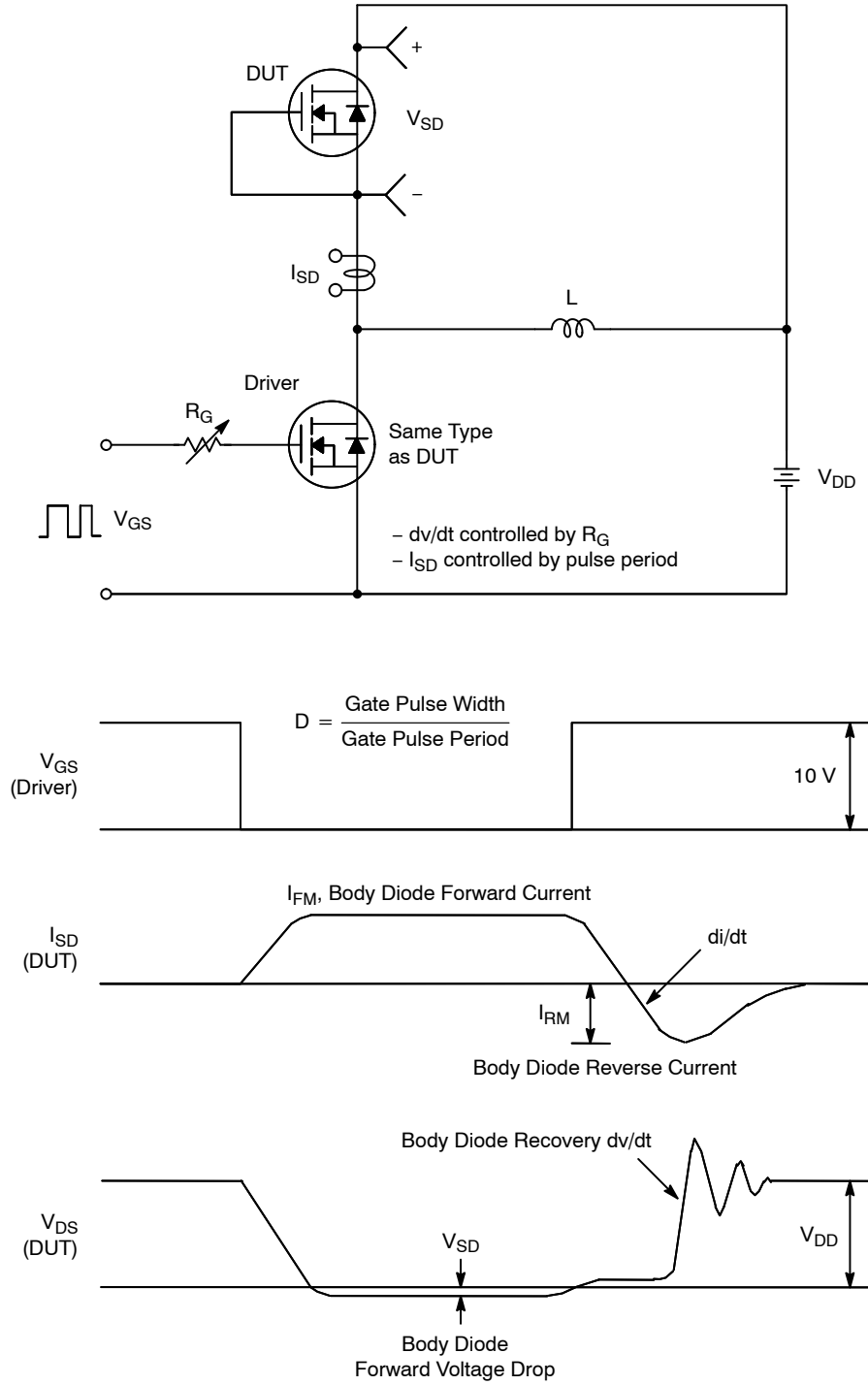


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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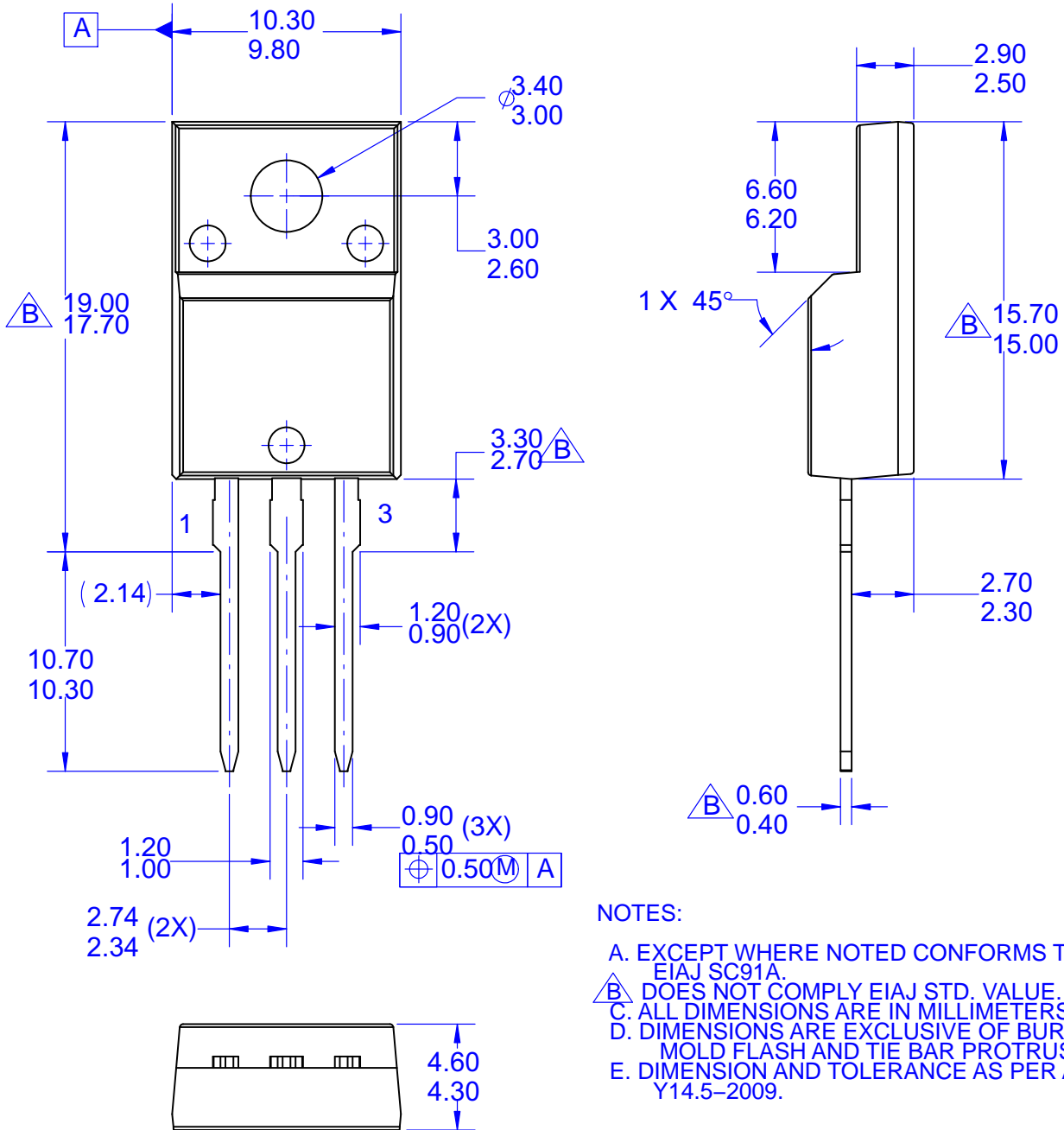
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



TO-220 FULLPAK 3LD
CASE 340BF
ISSUE O

DATE 31 AUG 2016



NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.

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