

## 21V to 60V<sub>IN</sub>, 150W, Cool-Power ZVS Buck-Boost Regulator

### Product Description

The PI3741-0x series is a high efficiency, wide range DC-DC ZVS Buck-Boost Regulator with two output range configurations that utilize the same high density System-in-Package (SiP). Integrating controller, power switches, support components and a high performance Zero-Voltage Switching (ZVS) topology within the PI3741-0x increases point of load performance while providing best in class power efficiency.

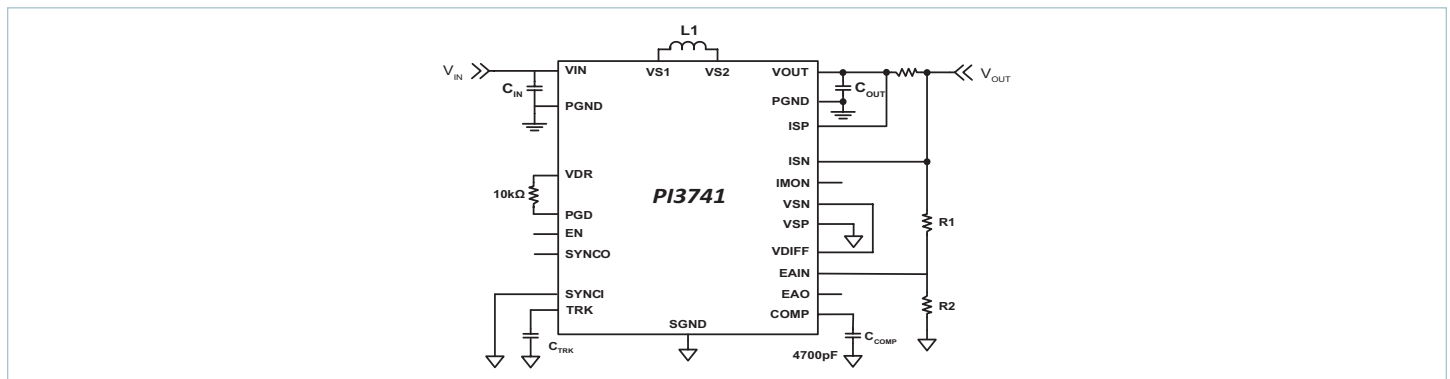
The PI3741-0x requires an external inductor, resistive divider and minimal capacitors to form a complete DC-DC switching mode buck-boost regulator.

| Device                         | Output Voltage |           |
|--------------------------------|----------------|-----------|
|                                | Set            | Range     |
| <a href="#">PI3741-00-LGIZ</a> | 24V            | 21 to 36V |
| <a href="#">PI3741-01-LGIZ</a> | 48V            | 36 to 54V |

The ZVS architecture also enables high frequency operation while minimizing switching losses and maximizing efficiency. The high switching frequency operation reduces the size of the external filtering components, improves power density, and enables fast dynamic response to line and load transients.



### Typical Application



### Features & Benefits

- Up to 97% efficiency
- 150W of continuous output power (for specific conditions)
- Fast transient response
- Parallel capable with single wire current sharing
- External frequency synchronization / interleaving
- High Side Current Sense Amplifier
- General Purpose Amplifier
- Input Over/Undervoltage Lockout (OVLO/UVLO)
- Output Overvoltage Protection (OVP)
- Over Temperature Protection (OTP)
- Fast and slow current limits
- -40°C to 115°C operating range (T<sub>J</sub>)
- Excellent light load efficiency

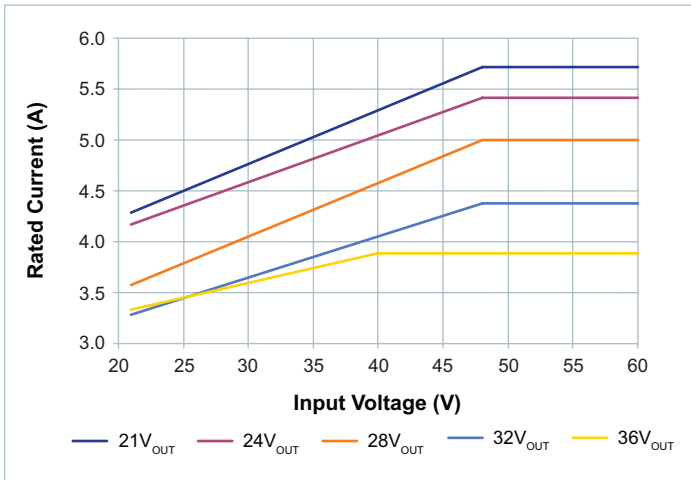
### Applications

- Telecom, Networking, Lighting
- Computing, Communications, Industrial
- Renewable Energy Systems

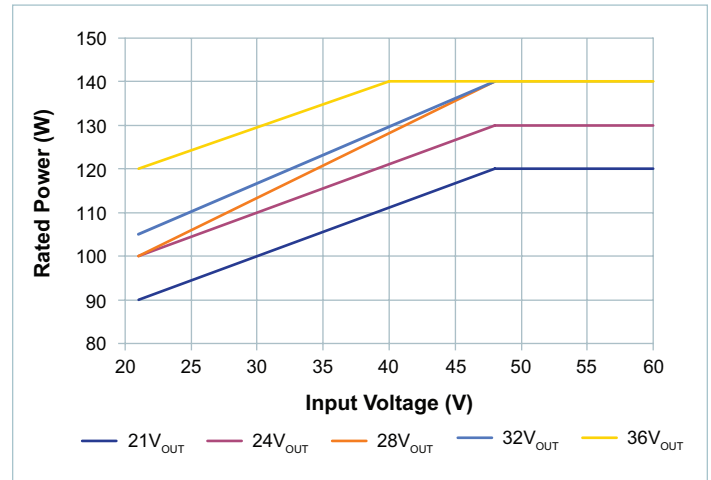
### Package Information

- 10mm x 14mm x 2.56mm LGA SiP

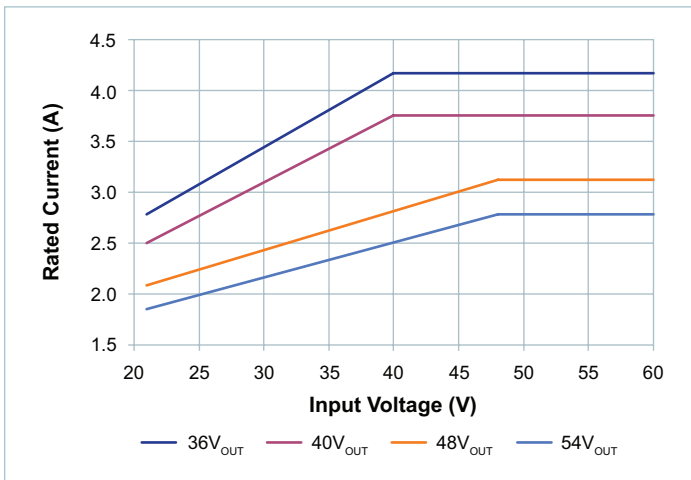
Rated Output Current / Power



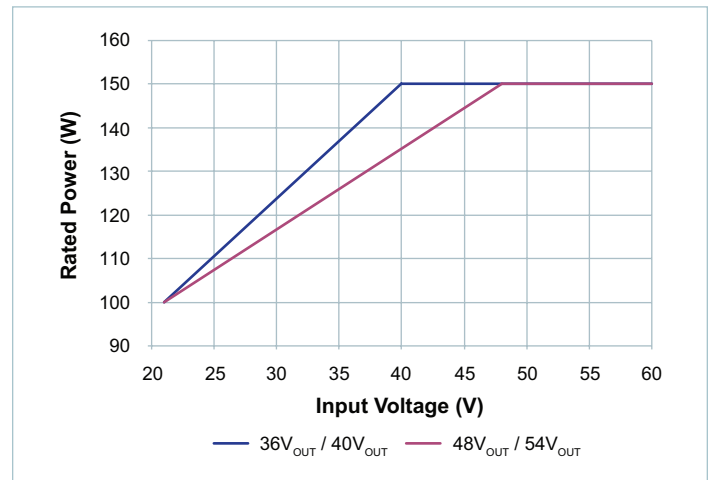
Output Current of PI3741-00-LGIZ



Output Power of PI3741-00-LGIZ



Output Current of PI3741-01-LGIZ



Output Power of PI3741-01-LGIZ

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## Order Information

| Part Number    | Description                                       | Package                 | Transport Media | MFG   |
|----------------|---|-------------------------|-----------------|-------|
| PI3741-00-LGIZ | 21 – 60V <sub>IN</sub> to 21 – 36V <sub>OUT</sub> | 10mm x 14mm 108-pin LGA | TRAY            | Vicor |
| PI3741-01-LGIZ | 21 – 60V <sub>IN</sub> to 36 – 54V <sub>OUT</sub> | 10mm x 14mm 108-pin LGA | TRAY            | Vicor |

## Absolute Maximum Ratings

**Note:** Stresses beyond these limits may cause permanent damage to the device. Operation at these conditions or conditions beyond those listed in the Electrical Specifications table is not guaranteed. All voltage nodes are referenced to PGND unless otherwise noted.

| Location              | Name               | V <sub>MAX</sub> | V <sub>MIN</sub>    | I <sub>SOURCE</sub> | I <sub>SINK</sub>  |
|-----------------------|--------------------|------------------|---------------------|---------------------|--------------------|
| 1–2, G–K              | V <sub>IN</sub>    | 75V              | -0.3V               | 40A <sup>[1]</sup>  | 40A <sup>[1]</sup> |
| 4–5, G–K              | VS1                | 75V              | -0.7V <sub>DC</sub> | 40A <sup>[1]</sup>  | 18A <sup>[1]</sup> |
| 10–11, G–K            | VS2                | 75V              | -0.7V <sub>DC</sub> | 40A <sup>[1]</sup>  | 18A <sup>[1]</sup> |
| 13–14, G–K            | V <sub>OUT</sub>   | 75V              | -0.7V <sub>DC</sub> | 40A <sup>[1]</sup>  | 40A <sup>[1]</sup> |
| 1E                    | VDR                | 5.5V             | -0.3V               | 30mA                | 200mA              |
| 1D                    | PGD                | 5.5V             | -0.3V               | 20mA                | 20mA               |
| 1C                    | SYNCO              | 5.5V             | -0.3V               | 5mA                 | 5mA                |
| 1B                    | SYNCI              | 5.5V             | -0.3V               | 5mA                 | 5mA                |
| 1A                    | FT1                | 5.5V             | -0.3V               | 5mA                 | 5mA                |
| 2A                    | FT2                | 5.5V             | -0.3V               | 5mA                 | 5mA                |
| 3A                    | FT3                | 5.5V             | -0.3V               | 5mA                 | 5mA                |
| 4A                    | FT4                | 5.5V             | -0.3V               | 10mA                | 10mA               |
| 5A                    | EN                 | 5.5V             | -0.3V               | 5mA                 | 5mA                |
| 6A                    | TRK                | 5.5V             | -0.3V               | 50mA                | 50mA               |
| 7A                    | LGH                | 5.5V             | -0.3V               | 5mA                 | 5mA                |
| 8A                    | COMP               | 5.5V             | -0.3V               | 5mA                 | 5mA                |
| 9A                    | VSN                | 5.5V             | -1.5V               | 5mA                 | 5mA                |
| 10A                   | VSP                | 5.5V             | -1.5V               | 5mA                 | 5mA                |
| 11A                   | VDIFF              | 5.5V             | -0.5V               | 5mA                 | 5mA                |
| 12A                   | EAIN               | 5.5V             | -0.3V               | 5mA                 | 5mA                |
| 13A                   | EAO                | 5.5V             | -0.3V               | 5mA                 | 5mA                |
| 14A                   | IMON               | 5.5V             | -0.3V               | 5mA                 | 5mA                |
| 14D                   | ISN <sup>[2]</sup> | 75V              | -2V <sub>DC</sub>   | 5mA                 | 5mA                |
| 14E                   | ISP <sup>[2]</sup> | 75V              | -2V <sub>DC</sub>   | 5mA                 | 5mA                |
| 10–14, B + 10–12, C–E | SGND               | 0.3V             | -0.3V               | 200mA               | 200mA              |
| 2–9, B–E + 7–8, F–K   | PGND               | N/A              | N/A                 | 18A <sup>[1]</sup>  | 18A <sup>[1]</sup> |

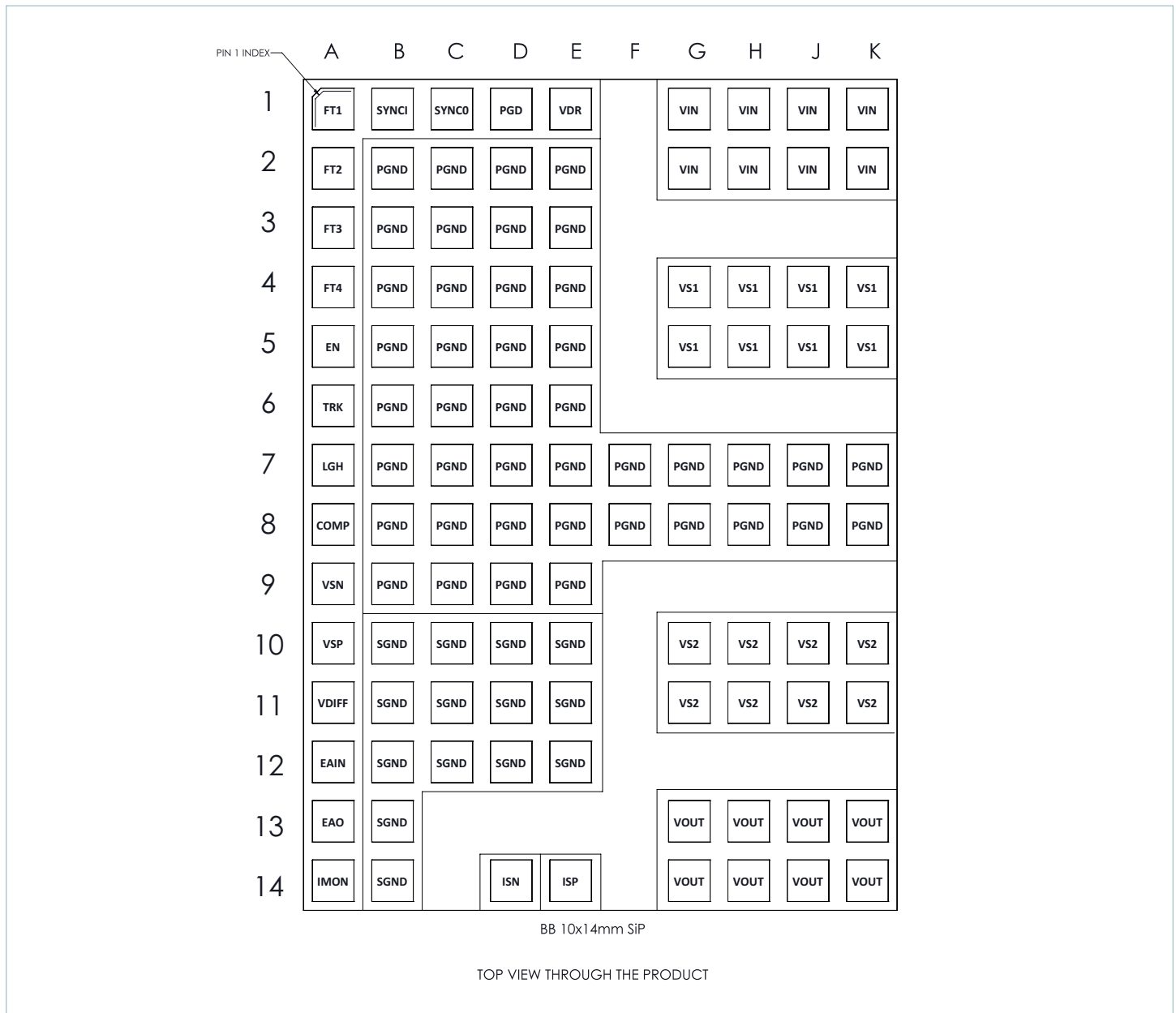
<sup>[1]</sup> Non-Operating Test Mode Limits.

<sup>[2]</sup> The ISP pin to ISN pin has a maximum differential limit of +5.5V<sub>DC</sub> and -0.5V<sub>DC</sub>.

## Pin Description

| Pin Number            | Pin Name | Description  |
|-----------------------|----------|--|
| 1–2, G–K              | VIN      | Input voltage and sense node for UVLO, OVLO and feed forward compensation.   |
| 4–5, G–K              | VS1      | Input side switching node and ZVS sense node for power switches.   |
| 10–11, G–K            | VS2      | Output side switching node and ZVS sense node for power switches.  |
| 13–14, G–K            | VOUT     | Output voltage and sense node for power switches, $V_{OUT}$ feed forward compensation, $V_{OUT\_OV}$ and internal signals.   |
| 1E                    | VDR      | Internal 5.1V supply for gate drivers and internal logic. May be used as reference or low power bias supply for up to 2mA. Must be impedance limited by the user.  |
| 1D                    | PGD      | Fault & Power Good indicator. PGD pulls low when the regulator is not operating or if EAIN is less than 1.4V.  |
| 1C                    | SYNCO    | Synchronization output. Outputs a high signal for $\frac{1}{2}$ of the programmed switching period at the beginning of each switching cycle, for synchronization of other regulators.  |
| 1B                    | SYNCI    | Synchronization input. When a falling edge synchronization pulse is detected, the PI3741-0x will delay the start of the next switching cycle until the next falling edge sync pulse arrives, up to a maximum delay of two times the programmed switching period. If the next pulse does not arrive within two times the programmed switching period, the controller will leave sync mode and start a switching cycle automatically. Connect to SGND when not in use. |
| 1A                    | FT1      | For factory use only. Connect to SGND or leave floating in application.  |
| 2A                    | FT2      | For factory use only. Connect to SGND or leave floating in application.  |
| 3A                    | FT3      | For factory use only. Connect to SGND in application.  |
| 4A                    | FT4      | For factory use only. Connect to SGND in application.  |
| 5A                    | EN       | Regulator Enable control. Asserted high or left floating – regulator enabled; Asserted low, regulator output disabled.   |
| 6A                    | TRK      | Soft-start and track input. An external capacitor may be connected between TRK pin and SGND to decrease the rate of output rise during soft-start.   |
| 7A                    | LGH      | For factory use only. Connect to SGND in application.  |
| 8A                    | COMP     | Error amp compensation dominant pole. Connect a capacitor of 4700pF by default between COMP and SGND to set the control loop dominant pole. If the application requires output capacitance from recommended in table 1, please contact Applications Support to compensate the control loop.  |
| 9A                    | VSN      | General purpose amplifier inverting input.   |
| 10A                   | VSP      | General purpose amplifier non-inverting input.   |
| 11A                   | VDIFF    | General Purpose amplifier output. When unused connect VDIFF to VSN and VSP to SGND.  |
| 12A                   | EAIN     | Error amplifier inverting input and sense for PGD. Connect by resistive divider to the output.   |
| 13A                   | EAO      | Error amp output: External connection for additional compensation and current sharing. Leave floating to use the internal error amplifier capacitance for default loop compensation. Please contact Applications Support if additional compensation is needed.   |
| 14A                   | IMON     | High side current sense amplifier output.  |
| 14D                   | ISN      | High side current sense amplifier negative input.  |
| 14E                   | ISP      | High side current sense amplifier positive input.  |
| 10–14, B + 10–12, C–E | SGND     | Signal ground. Internal logic and analog ground for the regulator. SGND and PGND are star connected within the regulator package.  |
| 2–9, B–E + 7–8, F–K   | PGND     | Power ground. $V_{IN}$ , $V_{OUT}$ , VS1 and VS2 power returns. SGND and PGND are star connected within the regulator package.   |

Package Pin-Out



Large Pin Blocks

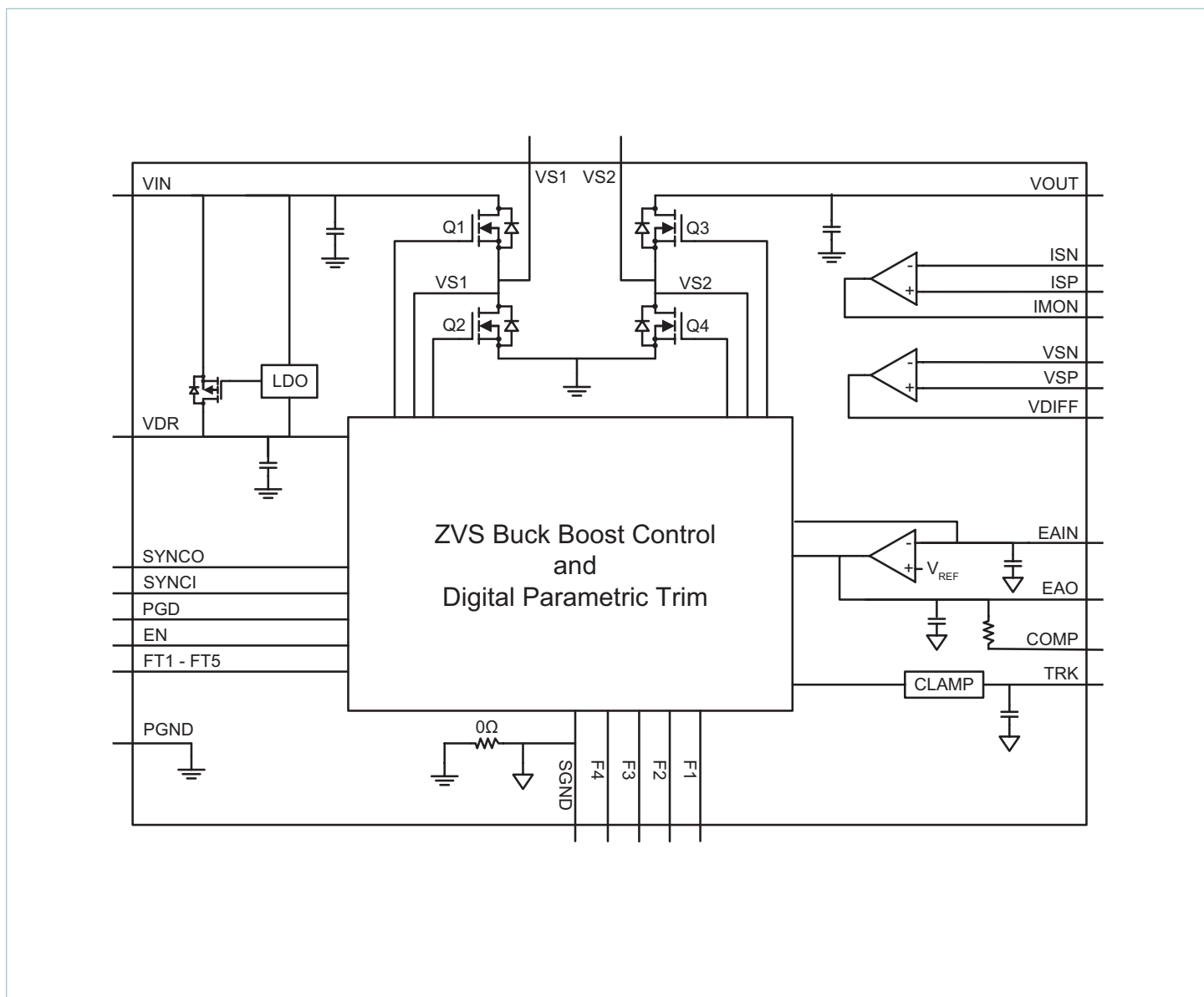
| Pin Block Name | Group of pins  |
|----------------|--|
| VIN            | G1-2, H1-2, J1-2, K1-2                               |
| VS1            | G4-5, H4-5, J4-5, K4-5                               |
| PGND           | B2-9, C2-9, D2-9, E2-9, F7-8, G7-8, H7-8, J7-8, K7-8 |
| VS2            | G10-11, H10-11, J10-11, K10-11                       |
| VOUT           | G13-14, H13-14, J13-14, K13-14                       |
| SGND           | B10-14, C10-12, D10-12, E10-12                       |

### Storage and Handling Information

|  |                      |
|--|----------------------|
| Maximum Storage Temperature Range            | -65°C to 150°C       |
| Maximum Operating Junction Temperature Range | -40°C to 115°C       |
| Soldering Temperature for 20 seconds         | 245°C                |
| MSL Rating                                   | 3                    |
| ESD Rating <sup>[3]</sup>                    | 2.0kV HBM; 1.0kV CDM |

<sup>[3]</sup> JS-200-2014, JESD22-A114F.

### Block Diagram



## PI3741-00-LGIZ Electrical Characteristics

Specifications apply for the conditions  $-40^{\circ}\text{C} < T_J < 115^{\circ}\text{C}$ ,  $V_{IN} = 48\text{V}$ ,  $V_{OUT} = 24\text{V}$ ,  $L_{EXT} = 900\text{nH}$  [4], external  $C_{IN} = 5 \times 2.2\mu\text{F}$ , external  $C_{OUT} = 8 \times 2.2\mu\text{F}$ , unless otherwise noted.

| Parameter   | Symbol                           | Conditions  | Min   | Typ  | Max   | Unit              |
|---|----------------------------------|---|-------|------|-------|-------------------|
| <b>Input Specifications</b>   |                                  |   |       |      |       |                   |
| Input Voltage   | $V_{IN\_DC}$                     |   | 21    | 48   | 60    | V                 |
| Input Current During Output Short (Fault Condition Duty Cycle)                | $I_{IN\_SHORT}$                  | [5]   |       | 1.9  |       | mA                |
| Input Quiescent Current   | $I_{Q\_VIN}$                     | Enabled (no load)   |       | 4    |       | mA                |
| Input Quiescent Current   | $I_{Q\_VIN}$                     | Disabled  |       | 1.5  |       | mA                |
| Input Voltage Slew Rate   | $V_{IN\_SR}$                     | [5]   |       |      | 1     | V / $\mu\text{s}$ |
| Internal Input Capacitance  | $C_{IN}$                         | $25^{\circ}\text{C}$ , $V_{IN} = 48\text{V}$  |       | 0.5  |       | $\mu\text{F}$     |
| $V_{IN}$ UVLO Threshold Rising  | $V_{IN\_UVLO\_START}$            |   |       | 19.2 |       | V                 |
| $V_{IN}$ UVLO Hysteresis  | $V_{IN\_UVLO\_HYS}$              |   |       | 0.7  |       | V                 |
| $V_{IN}$ OVLO Threshold Rising  | $V_{IN\_OVLO\_START}$            |   | 61    | 64.5 | 68    | V                 |
| $V_{IN}$ OVLO Hysteresis  | $V_{IN\_OVLO\_HYS}$              |   |       | 1.3  |       | V                 |
| <b>Output Specifications</b>  |                                  |   |       |      |       |                   |
| EAIN Voltage Total Regulation   | $V_{EAIN\_DC}$                   |   | 1.667 | 1.7  | 1.734 | V                 |
| Output Voltage Range  | $V_{OUT\_DC}$                    |   | 21    | 24   | 36    | V                 |
| Output Current Range  | $I_{OUT\_DCR}$                   | [6]   | 0     |      | max   | A                 |
| Output Current Steady State   | $I_{OUT\_DC}$                    | $V_{IN} = 21 - 48\text{V}$ , $V_{OUT} \leq 24\text{V}$ , $T_{CASE} = 25^{\circ}\text{C}$ [6]  | 4.17  |      |       | A                 |
|   |                                  | $V_{IN} = 48 - 60\text{V}$ , $V_{OUT} \leq 24\text{V}$ , $T_{CASE} = 25^{\circ}\text{C}$ [6]  | 5.42  |      |       |                   |
| Output Power Steady State   | $P_{OUT\_DC}$                    | $V_{IN} = 21 - 48\text{V}$ , $V_{OUT} = 24 - 36\text{V}$ , $T_{CASE} = 25^{\circ}\text{C}$ [6]  | 100   |      |       | W                 |
|   |                                  | $V_{IN} = 48 - 60\text{V}$ , $V_{OUT} = 24 - 36\text{V}$ , $T_{CASE} = 25^{\circ}\text{C}$ [6]  | 130   |      |       |                   |
| Line Regulation   | $\Delta V_{OUT}(\Delta V_{IN})$  | @ $25^{\circ}\text{C}$ , $21\text{V} < V_{IN} < 60\text{V}$   |       | 0.10 |       | %                 |
| Load Regulation   | $\Delta V_{OUT}(\Delta I_{OUT})$ | @ $25^{\circ}\text{C}$ , $I_{OUT}$ above 5% of the typical full load  |       | 0.10 |       | %                 |
| Output Ripple   | $V_{OUT\_AC}$                    | $I_{OUT} = 5.8\text{A}$ , $V_{IN} = 48\text{V}$ , $V_{OUT} = 24\text{V}$ , $T_{CASE} = 25^{\circ}\text{C}$<br>$C_{OUT\_EX} = 8 \times 2.2\mu\text{F}$ , 100V, X7R, 20MHz BW |       | 208  |       | mVp-p             |
| Internal Output Capacitance   | $C_{OUT}$                        | $25^{\circ}\text{C}$ , $V_{OUT} = 24\text{V}$   |       | 0.75 |       | $\mu\text{F}$     |
| $V_{OUT}$ Overvoltage Threshold   | $V_{OUT\_OVT}$                   | Rising $V_{OUT}$ threshold to detect open loop  | 39.8  | 41.9 | 44    | V                 |
| $V_{OUT}$ Overvoltage Hysteresis  | $V_{OUT\_OVH}$                   |   |       | 0.8  |       | V                 |
| <b>VDR</b>  |                                  |   |       |      |       |                   |
| $V_{DR}$ Supply Voltage   | $V_{DR}$                         | Generated internally  | 4.9   | 5.1  | 5.36  | V                 |
| <b>Current Sense Amplifier (Dedicated to monitor Input or Output Current)</b> |                                  |   |       |      |       |                   |
| ISP Pin Bias Current (Sink)   |                                  | $V_{OUT} = 10\text{V}$ , Flows to SGND  | 90    | 150  | 260   | $\mu\text{A}$     |
| ISN Pin Bias Current  |                                  | $V_{OUT} = 10\text{V}$  |       | 0    |       | $\mu\text{A}$     |
| Common Mode Input Range   |                                  |   | 8     |      | 60    | V                 |
| IMON Source Current   |                                  |   | 1     | 1.8  | 3     | mA                |
| IMON Sink Current   |                                  |   | 1     | 1.6  | 2.6   | mA                |
| IMON Output At No Load  |                                  |   | 0     |      | 10    | mV                |
| Full Scale Error  |                                  | 40mV input  | -4    |      | 4     | %                 |
| Bandwidth   |                                  | [5]   |       | 40   |       | kHz               |
| Settling Time For Full Scale Step   |                                  | 1%  |       | 20   |       | $\mu\text{s}$     |
| Gain  | $A_{V\_CS}$                      |   |       | 20   |       | V / V             |



## PI3741-00-LGIZ Electrical Characteristics (Cont.)

Specifications apply for the conditions  $-40^{\circ}\text{C} < T_J < 115^{\circ}\text{C}$ ,  $V_{\text{IN}} = 48\text{V}$ ,  $V_{\text{OUT}} = 24\text{V}$ ,  $L_{\text{EXT}} = 900\text{nH}$  [4], external  $C_{\text{IN}} = 5 \times 2.2\mu\text{F}$ , external  $C_{\text{OUT}} = 8 \times 2.2\mu\text{F}$ , unless otherwise noted.

| Parameter                                      | Symbol                   | Conditions  | Min   | Typ   | Max                           | Unit               |
|--|--------------------------|---|-------|-------|-------------------------------|--------------------|
| <b>General Purpose Amplifier</b>               |                          |   |       |       |                               |                    |
| Open Loop Gain                                 |                          | [5]   | 96    | 120   | 140                           | dB                 |
| Small Signal Gain-Bandwidth                    |                          | [5]   | 5     | 7     | 12                            | MHz                |
| Offset   |                          |   | -1    |       | 1                             | mV                 |
| Common Mode Input Range                        |                          |   | -0.1  |       | 2.5                           | V                  |
| Differential Mode Input Range                  |                          |   |       |       | 2                             | V                  |
| Maximum Output Voltage                         |                          | IDIFF = -1mA  |       |       | $V_{\text{DR}} - 0.2\text{V}$ | V                  |
| Minimum Output Voltage                         |                          | No Load   |       |       | 20                            | mV                 |
| Capacitive Load for Stable Operation           |                          | [5]   | 0     |       | 100                           | pF                 |
| Slew Rate                                      |                          |   |       | 10    |                               | V / $\mu\text{s}$  |
| Output Current                                 |                          |   | -1    |       | 1                             | mA                 |
| <b>Transconductance Error Amplifier</b>        |                          |   |       |       |                               |                    |
| Reference                                      | $V_{\text{REF}}$         | EAIN = EAO, 25°C  | 1.688 | 1.7   | 1.712                         | V                  |
|  |                          | EAIN = EAO  | 1.674 | 1.7   | 1.726                         |                    |
| Input Range                                    | $V_{\text{EAIN}}$        | Note $V_{\text{EAIN\_OV}}$ below                                | 0     |       | $V_{\text{DR}}$               | V                  |
| Maximum Output Voltage                         |                          |   | 3.35  | 3.6   | 4.0                           | V                  |
| Minimum Output Voltage                         |                          |   |       | 0.05  | 0.15                          | V                  |
| Transconductance                               |                          | Factory Set   |       | 7.6   |                               | mS                 |
| Zero Resistor                                  |                          | Factory Set   |       | 6     |                               | k $\Omega$         |
| EAO Output Current Sourcing                    |                          | $V_{\text{EAO}} = 50\text{mV}$ , $V_{\text{EAIN}} = 0\text{V}$  |       | 400   |                               | $\mu\text{A}$      |
| EAO Output Current Sinking                     |                          | $V_{\text{EAO}} = 2\text{V}$ , $V_{\text{EAIN}} = 5\text{V}$    |       | 400   |                               | $\mu\text{A}$      |
| Open Loop Gain                                 |                          | $R_{\text{OUT}} > 1\text{M}\Omega$ [5]                          | 70    | 80    |                               | dB                 |
| Input Capacitance                              |                          |   |       | 56    |                               | pF                 |
| Output Capacitance                             |                          |   |       | 56    |                               | pF                 |
| <b>Control and Protection</b>                  |                          |   |       |       |                               |                    |
| Switching Frequency                            | $F_{\text{SW}}$          |   |       | 1     |                               | MHz                |
| $V_{\text{EAO}}$ Pulse Skip Threshold          | $V_{\text{EAO\_PST}}$    | $V_{\text{EAO}}$ to SGND  |       | 0.4   |                               | V                  |
| Control Node Range                             | $V_{\text{RAMP}}$        |   | 0     |       | 3.3                           | V                  |
| $V_{\text{EAO}}$ Overload Threshold            | $V_{\text{EAO\_OL}}$     | $V_{\text{EAO}}$ to SGND  | 3.175 | 3.3   | 3.425                         | V                  |
| Overload Timeout                               | $T_{\text{OL}}$          | $V_{\text{EAO}} > V_{\text{EAO\_OL}}$                           |       | 1     |                               | ms                 |
| Overload due to EAO limit                      | $I_{\text{OUT\_EAOLIM}}$ | Module shuts down after 1ms of overload and restarts after 30ms |       | 6.8   |                               | A                  |
| $V_{\text{EAIN}}$ Output Overvoltage Threshold | $V_{\text{EAIN\_OV}}$    | $V_{\text{EAIN}} > V_{\text{EAIN\_OV}}$                         | 1.94  | 2.04  | 2.14                          | V                  |
| Overtemperature Fault Threshold                | $T_{\text{OTP}}$         | [5]   |       | 125   |                               | $^{\circ}\text{C}$ |
| Overtemperature Restart Hysteresis             | $T_{\text{OPT\_HYS}}$    | [5]   |       | 30    |                               | $^{\circ}\text{C}$ |
| $V_{\text{OUT}}$ Negative Fault Threshold      |                          |   | -0.45 | -0.25 | -0.15                         | V                  |

## PI3741-00-LGIZ Electrical Characteristics (Cont.)

Specifications apply for the conditions  $-40^{\circ}\text{C} < T_J < 115^{\circ}\text{C}$ ,  $V_{\text{IN}} = 48\text{V}$ ,  $V_{\text{OUT}} = 24\text{V}$ ,  $L_{\text{EXT}} = 900\text{nH}$  <sup>[4]</sup>, external  $C_{\text{IN}} = 5 \times 2.2\mu\text{F}$ , external  $C_{\text{OUT}} = 8 \times 2.2\mu\text{F}$ , unless otherwise noted.

| Parameter                               | Symbol                     | Conditions   | Min                   | Typ      | Max             | Unit          |
|---|----------------------------|--|-----------------------|----------|-----------------|---------------|
| <b>Soft Start and Tracking Function</b> |                            |  |                       |          |                 |               |
| TRK Active Range                        |                            | Nominal  | 0                     |          | 1.7             | V             |
| TRK Disable Threshold                   |                            |  | 20                    | 45       | 70              | mV            |
| TRK Internal Capacitance                |                            |  |                       | .047     |                 | $\mu\text{F}$ |
| Soft Start Charge Current               |                            |  | 30                    | 50       | 70              | $\mu\text{A}$ |
| Soft Start Discharge Current            |                            | $V_{\text{TRK}} = 0.5\text{V}$                             |                       | 9        |                 | mA            |
| Soft Start Time                         | $t_{\text{SS}}$            | Ext $C_{\text{SS}} = 0\mu\text{F}$                         |                       | 1.6      |                 | ms            |
| <b>Enable</b>                           |                            |  |                       |          |                 |               |
| Enable High Threshold                   | $\text{EN}_{\text{IH}}$    |  | 0.9                   | 1        | 1.1             | V             |
| Enable Low Threshold                    | $\text{EN}_{\text{IL}}$    |  | 0.7                   | 0.8      | 0.9             | V             |
| Enable Threshold Hysteresis             | $\text{EN}_{\text{HYS}}$   |  | 100                   | 200      | 300             | mV            |
| Enable Pin Bias Current                 |                            | $V_{\text{EN}} = 0\text{V}$ or $V_{\text{EN}} = 2\text{V}$ |                       | $\pm 50$ |                 | $\mu\text{A}$ |
| Enable Pull-up Voltage                  |                            | Floating   |                       | 2.0      |                 | V             |
| Fault Restart Delay Time                | $t_{\text{FR\_DLY}}$       |  |                       | 30       |                 | ms            |
| <b>Digital Signals</b>                  |                            |  |                       |          |                 |               |
| SYNCl High Threshold                    |                            | $V_{\text{DR}} = 5.1\text{V}$                              |                       | 1/2 VDR  |                 | V             |
| SYNCO High                              | $\text{SYNCO}_{\text{OH}}$ |  | $V_{\text{DR}} - 0.5$ |          | $V_{\text{DR}}$ | V             |
| SYNCO Low                               | $\text{SYNCO}_{\text{OL}}$ | $I_{\text{SYNCO}} = 1\text{mA}$                            |                       |          | 0.5             | V             |
| PGD High Leakage                        | $\text{PGD}_{\text{ILH}}$  | $V_{\text{PGD}} = V_{\text{DR}}$                           |                       |          | 10              | $\mu\text{A}$ |
| PGD Output Low                          | $\text{PGD}_{\text{OL}}$   | $I_{\text{PGD}} = 4\text{mA}$                              |                       |          | 0.4             | V             |
| PGD EAIN Low Rise                       |                            |  | 1.41                  | 1.45     | 1.48            | V             |
| PGD EAIN Low Fall                       |                            |  | 1.36                  | 1.41     | 1.46            | V             |
| PGD EAIN Threshold Hysteresis           |                            |  |                       | 35       |                 | mV            |
| PGD EAIN High                           |                            |  | 1.94                  | 2.04     | 2.14            | V             |

<sup>[4]</sup> See Inductor Pairing section.

<sup>[5]</sup> Assured to meet performance specification by design, test correlation, characterization, and / or statistical process control.

<sup>[6]</sup> Output current capability varies with input & output voltage. See rated output current / power curves on page 2.

## PI3741-01-LGIZ Electrical Characteristics

Specifications apply for the conditions  $-40^{\circ}\text{C} < T_J < 115^{\circ}\text{C}$ ,  $V_{IN} = 48\text{V}$ ,  $V_{OUT} = 48\text{V}$ ,  $L_{EXT} = 900\text{nH}$  [4], external  $C_{IN} = 5 \times 2.2\mu\text{F}$ , external  $C_{OUT} = 8 \times 2.2\mu\text{F}$ , unless otherwise noted.

| Parameter   | Symbol                           | Conditions  | Min   | Typ  | Max   | Unit              |
|---|----------------------------------|---|-------|------|-------|-------------------|
| <b>Input Specifications</b>   |                                  |   |       |      |       |                   |
| Input Voltage   | $V_{IN\_DC}$                     |   | 21    | 48   | 60    | V                 |
| Input Current During Output Short (Fault Condition Duty Cycle)                | $I_{IN\_SHORT}$                  | [5]   |       | 1.9  |       | mA                |
| Input Quiescent Current   | $I_{Q\_VIN}$                     | Enabled (no load)   |       | 5    |       | mA                |
| Input Quiescent Current   | $I_{Q\_VIN}$                     | Disabled  |       | 1.5  |       | mA                |
| Input Voltage Slew Rate   | $V_{IN\_SR}$                     | [5]   |       |      | 1     | V / $\mu\text{s}$ |
| Internal Input Capacitance  | $C_{IN}$                         | $25^{\circ}\text{C}$ , $V_{IN} = 48\text{V}$  |       | 0.5  |       | $\mu\text{F}$     |
| $V_{IN}$ UVLO Threshold Rising  | $V_{IN\_UVLO\_START}$            |   |       | 19.2 |       | V                 |
| $V_{IN}$ UVLO Hysteresis  | $V_{IN\_UVLO\_HYS}$              |   |       | 0.7  |       | V                 |
| $V_{IN}$ OVLO Threshold Rising  | $V_{IN\_OVLO\_START}$            |   | 61    | 64.5 | 68    | V                 |
| $V_{IN}$ OVLO Hysteresis  | $V_{IN\_OVLO\_HYS}$              |   |       | 1.3  |       | V                 |
| <b>Output Specifications</b>  |                                  |   |       |      |       |                   |
| EAIN Voltage Total Regulation   | $V_{EAIN\_DC}$                   |   | 1.667 | 1.7  | 1.734 | V                 |
| Output Voltage Range  | $V_{OUT\_DC}$                    |   | 36    | 48   | 54    | V                 |
| Output Current Range  | $I_{OUT\_DCR}$                   | [6]   | 0     |      | max   | A                 |
| Output Current Steady State   | $I_{OUT\_DC}$                    | $V_{IN} = 21 - 48\text{V}$ , $V_{OUT} \leq 48\text{V}$ , $T_{CASE} = 25^{\circ}\text{C}$ [6]  | 2.09  |      |       | A                 |
|   |                                  | $V_{IN} = 48 - 60\text{V}$ , $V_{OUT} \leq 48\text{V}$ , $T_{CASE} = 25^{\circ}\text{C}$ [6]  | 3.13  |      |       |                   |
| Output Power Steady State   | $P_{OUT\_DC}$                    | $V_{IN} = 21 - 48\text{V}$ , $V_{OUT} = 48 - 54\text{V}$ , $T_{CASE} = 25^{\circ}\text{C}$ [6]  | 100   |      |       | W                 |
|   |                                  | $V_{IN} = 48 - 60\text{V}$ , $V_{OUT} = 48 - 54\text{V}$ , $T_{CASE} = 25^{\circ}\text{C}$ [6]  | 150   |      |       |                   |
| Line Regulation   | $\Delta V_{OUT}(\Delta V_{IN})$  | @ $25^{\circ}\text{C}$ , $21\text{V} < V_{IN} < 60\text{V}$   |       | 0.10 |       | %                 |
| Load Regulation   | $\Delta V_{OUT}(\Delta I_{OUT})$ | @ $25^{\circ}\text{C}$ , $I_{OUT}$ above 5% of the typical full load  |       | 0.10 |       | %                 |
| Output Ripple   | $V_{OUT\_AC}$                    | $I_{OUT} = 4.2\text{A}$ , $V_{IN} = 48\text{V}$ , $V_{OUT} = 48\text{V}$ , $T_{CASE} = 25^{\circ}\text{C}$<br>$C_{OUT\_EX} = 8 \times 2.2\mu\text{F}$ , 100V, X7R, 20MHz BW |       | 320  |       | mVp-p             |
| Internal Output Capacitance   | $C_{OUT}$                        | $25^{\circ}\text{C}$ , $V_{OUT} = 48\text{V}$   |       | 0.5  |       | $\mu\text{F}$     |
| $V_{OUT}$ Overvoltage Threshold   | $V_{OUT\_OVT}$                   | Rising $V_{OUT}$ threshold to detect open loop  | 60    | 63.1 | 60.9  | V                 |
| $V_{OUT}$ Overvoltage Hysteresis  | $V_{OUT\_OVH}$                   |   |       | 1.3  |       | V                 |
| <b>VDR</b>  |                                  |   |       |      |       |                   |
| $V_{DR}$ Supply Voltage   | $V_{DR}$                         | Generated Internally  | 4.9   | 5.1  | 5.36  | V                 |
| <b>Current Sense Amplifier (Dedicated to monitor Input or Output Current)</b> |                                  |   |       |      |       |                   |
| ISP Pin Bias Current (Sink)   |                                  | $V_{OUT} = 10\text{V}$ , Flows to SGND  | 90    | 150  | 260   | $\mu\text{A}$     |
| ISN Pin Bias Current  |                                  | $V_{OUT} = 10\text{V}$  |       | 0    |       | $\mu\text{A}$     |
| Common Mode Input Range   |                                  |   | 8     |      | 60    | V                 |
| IMON Source Current   |                                  |   | 1     | 1.8  | 3     | mA                |
| IMON Sink Current   |                                  |   | 1     | 1.6  | 2.6   | mA                |
| IMON Output At No Load  |                                  |   | 0     |      | 10    | mV                |
| Full Scale Error  |                                  | 40mV input  | -4    |      | 4     | %                 |
| Bandwidth   |                                  | [5]   |       | 40   |       | kHz               |
| Settling Time For Full Scale Step   |                                  | 1%  |       | 20   |       | $\mu\text{s}$     |
| Gain  | $A_{V\_CS}$                      |   |       | 20   |       | V / V             |

## PI3741-01-LGIZ Electrical Characteristics (Cont.)

Specifications apply for the conditions  $-40^{\circ}\text{C} < T_J < 115^{\circ}\text{C}$ ,  $V_{\text{IN}} = 48\text{V}$ ,  $V_{\text{OUT}} = 48\text{V}$ ,  $L_{\text{EXT}} = 900\text{nH}$  [4], external  $C_{\text{IN}} = 5 \times 2.2\mu\text{F}$ , external  $C_{\text{OUT}} = 8 \times 2.2\mu\text{F}$ , unless otherwise noted.

| Parameter                                      | Symbol                   | Conditions  | Min   | Typ   | Max                           | Unit               |
|--|--------------------------|---|-------|-------|-------------------------------|--------------------|
| <b>General Purpose Amplifier</b>               |                          |   |       |       |                               |                    |
| Open Loop Gain                                 |                          | [5]   | 96    | 120   | 140                           | dB                 |
| Small Signal Gain-Bandwidth                    |                          | [5]   | 5     | 7     | 12                            | MHz                |
| Offset   |                          |   | -1    |       | 1                             | mV                 |
| Common Mode Input Range                        |                          |   | -0.1  |       | 2.5                           | V                  |
| Differential Mode Input Range                  |                          |   |       |       | 2                             | V                  |
| Maximum Output Voltage                         |                          | IDIFF = -1mA  |       |       | $V_{\text{DR}} - 0.2\text{V}$ | V                  |
| Minimum Output Voltage                         |                          | No Load   |       |       | 20                            | mV                 |
| Capacitive Load for Stable Operation           |                          | [5]   | 0     |       | 100                           | pF                 |
| Slew Rate                                      |                          |   |       | 10    |                               | V / $\mu\text{s}$  |
| Output Current                                 |                          |   | -1    |       | 1                             | mA                 |
| <b>Transconductance Error Amplifier</b>        |                          |   |       |       |                               |                    |
| Reference                                      | $V_{\text{REF}}$         | EAIN = EAO, 25°C  | 1.688 | 1.7   | 1.712                         | V                  |
|  |                          | EAIN = EAO  | 1.674 | 1.7   | 1.726                         |                    |
| Input Range                                    | $V_{\text{EAIN}}$        | Note $V_{\text{EAIN\_OV}}$ below                                | 0     |       | $V_{\text{DR}}$               | V                  |
| Maximum Output Voltage                         |                          |   | 3.35  | 3.6   | 4.0                           | V                  |
| Minimum Output Voltage                         |                          |   |       | 0.05  | 0.15                          | V                  |
| Transconductance                               |                          | Factory Set   |       | 5.1   |                               | mS                 |
| Zero Resistor                                  |                          | Factory Set   |       | 5     |                               | k $\Omega$         |
| EAO Output Current Sourcing                    |                          | $V_{\text{EAO}} = 50\text{mV}$ , $V_{\text{EAIN}} = 0\text{V}$  |       | 400   |                               | $\mu\text{A}$      |
| EAO Output Current Sinking                     |                          | $V_{\text{EAO}} = 2\text{V}$ , $V_{\text{EAIN}} = 5\text{V}$    |       | 400   |                               | $\mu\text{A}$      |
| Open Loop Gain                                 |                          | $R_{\text{OUT}} > 1\text{M}\Omega$ [5]                          | 70    | 80    |                               | dB                 |
| Input Capacitance                              |                          |   |       | 56    |                               | pF                 |
| Output Capacitance                             |                          |   |       | 56    |                               | pF                 |
| <b>Control and Protection</b>                  |                          |   |       |       |                               |                    |
| Switching Frequency                            | $F_{\text{SW}}$          |   |       | 1     |                               | MHz                |
| $V_{\text{EAO}}$ Pulse Skip Threshold          | $V_{\text{EAO\_PST}}$    | $V_{\text{EAO}}$ to SGND  |       | 0.4   |                               | V                  |
| Control Node Range                             | $V_{\text{RAMP}}$        |   | 0     |       | 3.3                           | V                  |
| $V_{\text{EAO}}$ Overload Threshold            | $V_{\text{EAO\_OL}}$     | $V_{\text{EAO}}$ to SGND  | 3.175 | 3.3   | 3.425                         | V                  |
| Overload Timeout                               | $T_{\text{OL}}$          | $V_{\text{EAO}} > V_{\text{EAO\_OL}}$                           |       | 1     |                               | ms                 |
| Overload due to EAO limit                      | $I_{\text{OUT\_EAOLIM}}$ | Module shuts down after 1ms of overload and restarts after 30ms |       | 5.0   |                               | A                  |
| $V_{\text{EAIN}}$ Output Overvoltage Threshold | $V_{\text{EAIN\_OV}}$    | $V_{\text{EAIN}} > V_{\text{EAIN\_OV}}$                         | 1.94  | 2.04  | 2.14                          | V                  |
| Overtemperature Fault Threshold                | $T_{\text{OTP}}$         | [5]   |       | 125   |                               | $^{\circ}\text{C}$ |
| Overtemperature Restart Hysteresis             | $T_{\text{OPT\_HYS}}$    | [5]   |       | 30    |                               | $^{\circ}\text{C}$ |
| $V_{\text{OUT}}$ Negative Fault Threshold      |                          |   | -0.45 | -0.25 | -0.15                         | V                  |

## PI3741-01-LGIZ Electrical Characteristics (Cont.)

Specifications apply for the conditions  $-40^{\circ}\text{C} < T_J < 115^{\circ}\text{C}$ ,  $V_{\text{IN}} = 48\text{V}$ ,  $V_{\text{OUT}} = 48\text{V}$ ,  $L_{\text{EXT}} = 900\text{nH}$  <sup>[4]</sup>, external  $C_{\text{IN}} = 5 \times 2.2\mu\text{F}$ , external  $C_{\text{OUT}} = 8 \times 2.2\mu\text{F}$ , unless otherwise noted.

| Parameter                               | Symbol                     | Conditions   | Min                   | Typ      | Max             | Unit          |
|---|----------------------------|--|-----------------------|----------|-----------------|---------------|
| <b>Soft Start and Tracking Function</b> |                            |  |                       |          |                 |               |
| TRK Active Range                        |                            | Nominal  | 0                     |          | 1.7             | V             |
| TRK Disable Threshold                   |                            |  | 20                    | 45       | 70              | mV            |
| TRK Internal Capacitance                |                            |  |                       | .047     |                 | $\mu\text{F}$ |
| Soft Start Charge Current               |                            |  | 30                    | 50       | 70              | $\mu\text{A}$ |
| Soft Start Discharge Current            |                            | $V_{\text{TRK}} = 0.5\text{V}$                             |                       | 9        |                 | mA            |
| Soft Start Time                         | $t_{\text{SS}}$            | Ext $C_{\text{SS}} = 0\mu\text{F}$                         |                       | 1.6      |                 | ms            |
| <b>Enable</b>                           |                            |  |                       |          |                 |               |
| Enable High Threshold                   | $\text{EN}_{\text{IH}}$    |  | 0.9                   | 1        | 1.1             | V             |
| Enable Low Threshold                    | $\text{EN}_{\text{IL}}$    |  | 0.7                   | 0.8      | 0.9             | V             |
| Enable Threshold Hysteresis             | $\text{EN}_{\text{HYS}}$   |  | 100                   | 200      | 300             | mV            |
| Enable Pin Bias Current                 |                            | $V_{\text{EN}} = 0\text{V}$ or $V_{\text{EN}} = 2\text{V}$ |                       | $\pm 50$ |                 | $\mu\text{A}$ |
| Enable Pull-up Voltage                  |                            | Floating   |                       | 2.0      |                 | V             |
| Fault Restart Delay Time                | $t_{\text{FR\_DLY}}$       |  |                       | 30       |                 | ms            |
| <b>Digital Signals</b>                  |                            |  |                       |          |                 |               |
| SYNCl High Threshold                    |                            | $V_{\text{DR}} = 5.1\text{V}$                              |                       | 1/2 VDR  |                 | V             |
| SYNCO High                              | $\text{SYNCO}_{\text{OH}}$ |  | $V_{\text{DR}} - 0.5$ |          | $V_{\text{DR}}$ | V             |
| SYNCO Low                               | $\text{SYNCO}_{\text{OL}}$ | $I_{\text{SYNCO}} = 1\text{mA}$                            |                       |          | 0.5             | V             |
| PGD High Leakage                        | $\text{PGD}_{\text{ILH}}$  | $V_{\text{PGD}} = V_{\text{DR}}$                           |                       |          | 10              | $\mu\text{A}$ |
| PGD Output Low                          | $\text{PGD}_{\text{OL}}$   | $I_{\text{PGD}} = 4\text{mA}$                              |                       |          | 0.4             | V             |
| PGD EAIN Low Rise                       |                            |  | 1.41                  | 1.45     | 1.48            | V             |
| PGD EAIN Low Fall                       |                            |  | 1.36                  | 1.41     | 1.46            | V             |
| PGD EAIN Threshold Hysteresis           |                            |  |                       | 35       |                 | mV            |
| PGD EAIN High                           |                            |  | 1.94                  | 2.04     | 2.14            | V             |

<sup>[4]</sup> See Inductor Pairing section.

<sup>[5]</sup> Assured to meet performance specification by design, test correlation, characterization, and/or statistical process control.

<sup>[6]</sup> Output current capability varies with input & output voltage. See rated output current / power curves on page 2.

PI3741-00-LGIZ Performance Characteristics  $T_A = 25^\circ\text{C}$

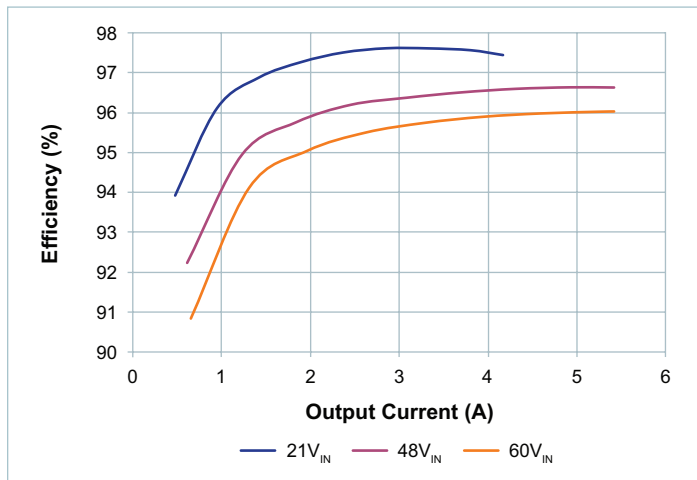


Figure 1 — 24V<sub>OUT</sub> Efficiency

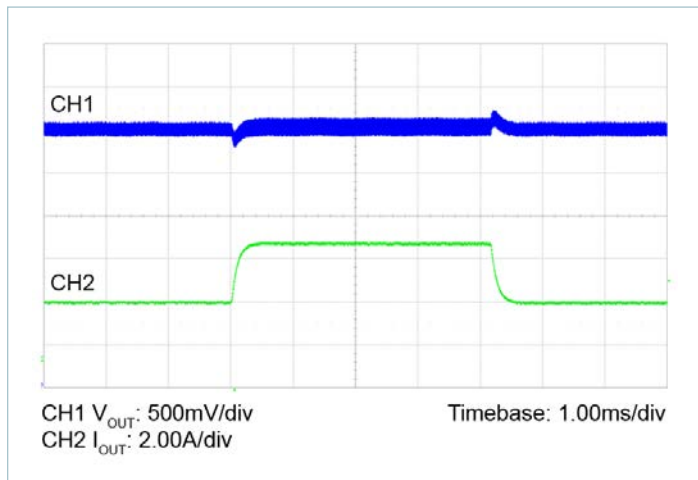


Figure 4 — 48V<sub>IN</sub> to 24V<sub>OUT</sub>,  $C_{OUT} = 8 \times 2.2\mu\text{F}$  Ceramic  
5.42A to 2.71A Load Step, 0.1A/ $\mu\text{s}$

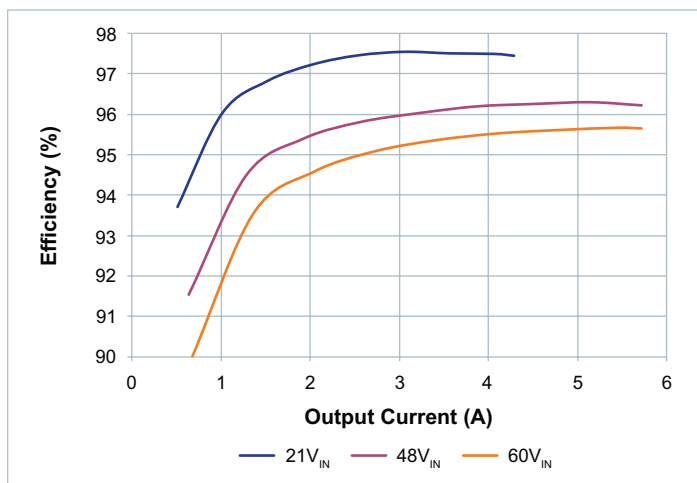


Figure 2 — 21V<sub>OUT</sub> Efficiency

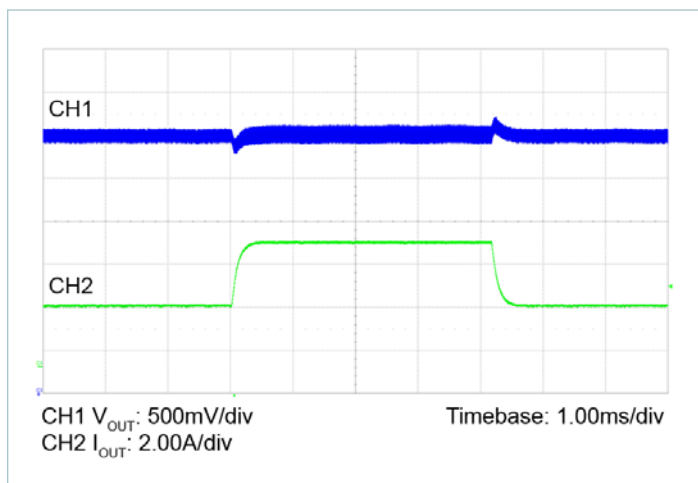


Figure 5 — 60V<sub>IN</sub> to 21V<sub>OUT</sub>,  $C_{OUT} = 8 \times 2.2\mu\text{F}$  Ceramic  
5.72A to 2.86A Load Step, 0.1A/ $\mu\text{s}$

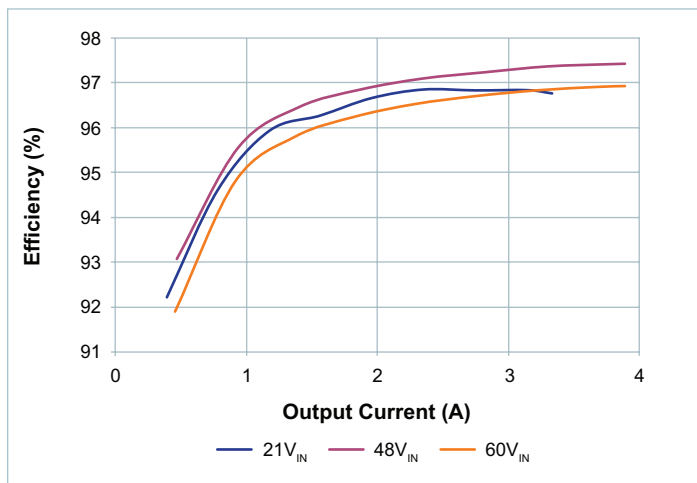


Figure 3 — 36V<sub>OUT</sub> Efficiency

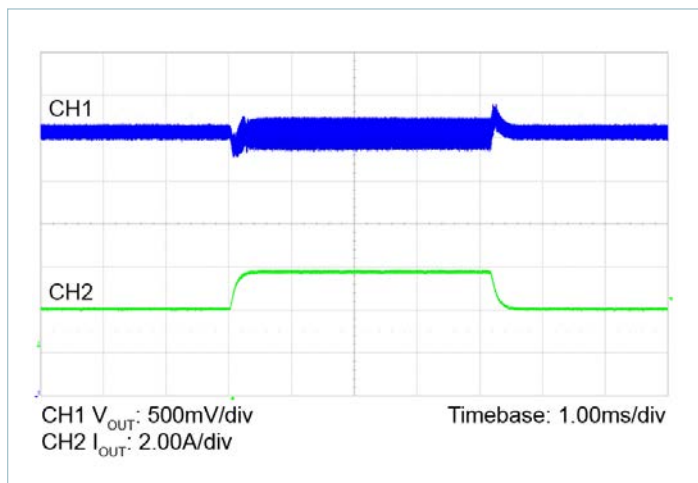


Figure 6 — 21V<sub>IN</sub> to 36V<sub>OUT</sub>,  $C_{OUT} = 8 \times 2.2\mu\text{F}$  Ceramic  
3.34A to 1.67A Load Step, 0.1A/ $\mu\text{s}$

PI3741-00-LGIZ Performance Characteristics  $T_A = 25^\circ\text{C}$  (Cont.)

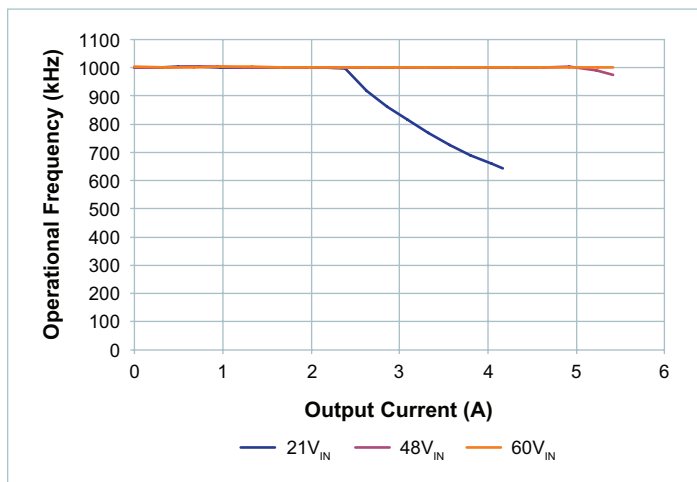


Figure 7 — Switching Frequency vs. Output Current @  $24V_{OUT}$

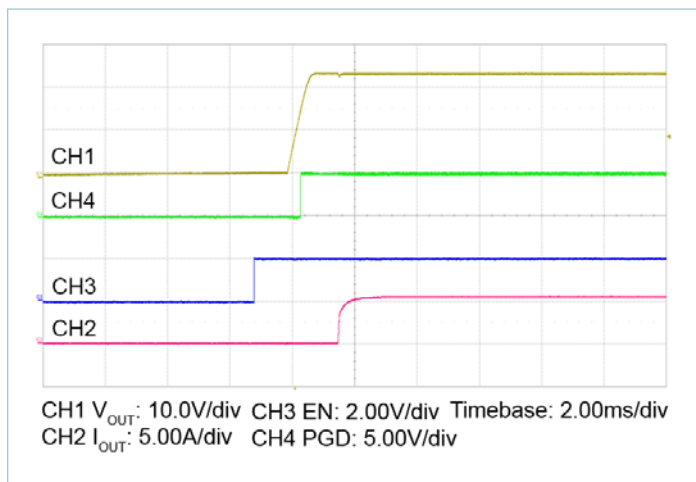


Figure 10 — Start-up with  $48V_{IN}$  to  $24V_{OUT}$  at  $5.42A$ ,  
 $Ext C_{SS} = 0\mu F$

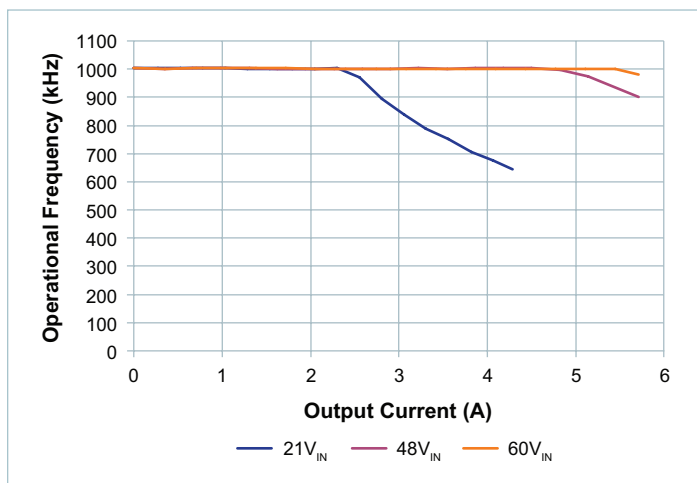


Figure 8 — Switching Frequency vs. Output Current @  $21V_{OUT}$

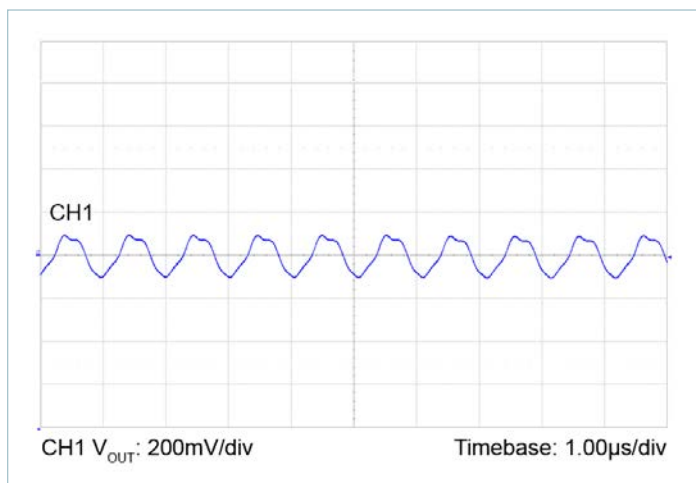


Figure 11 — Output voltage ripple at  $48V_{IN}$  to  $24V_{OUT}$ ,  $5.42A$ ;  
 $C_{OUT} = 8 \times 2.2\mu F$  Ceramic

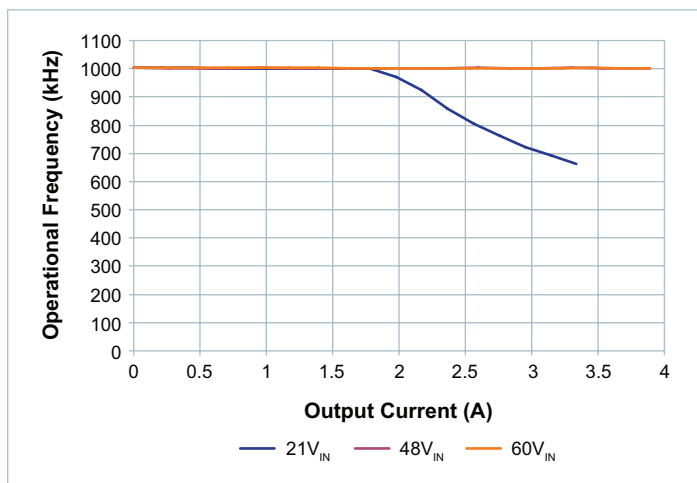


Figure 9 — Switching Frequency vs. Output Current @  $36V_{OUT}$

PI3741-00-LGIZ Efficiency & Power Loss  $T_A = 25^\circ\text{C}$  [7]

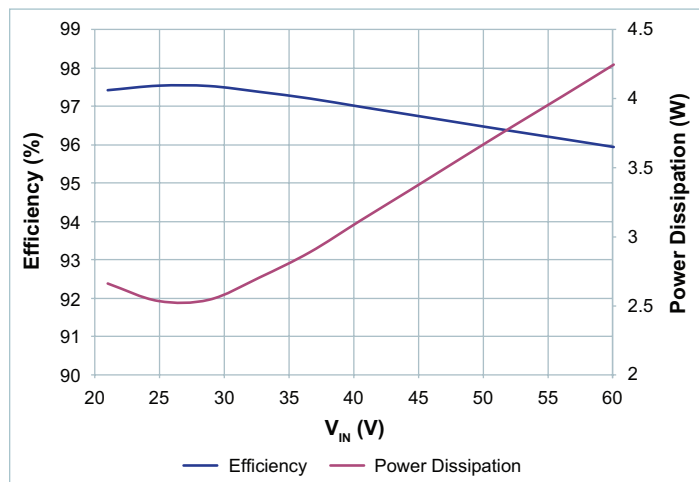


Figure 12 —  $24V_{OUT}$  Efficiency and Power Dissipation at 4.17A over input Voltage Range

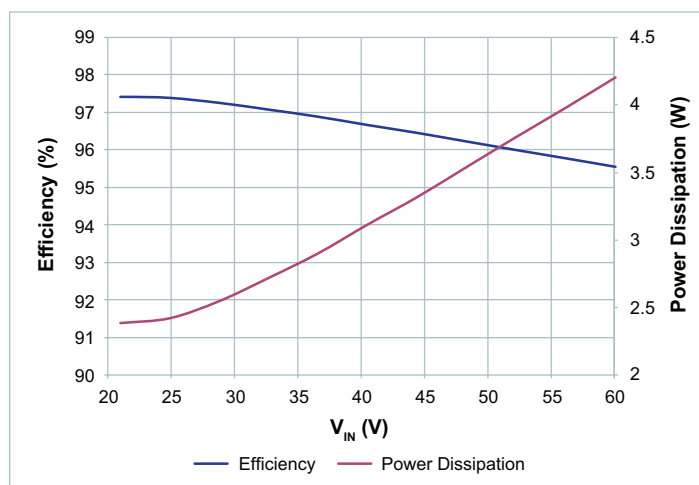


Figure 13 —  $21V_{OUT}$  Efficiency and Power Dissipation at 4.29A over input Voltage Range

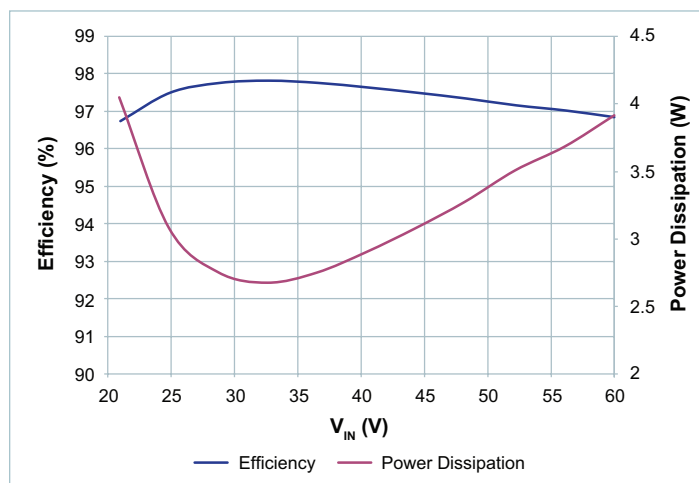


Figure 14 —  $36V_{OUT}$  Efficiency and Power Dissipation at 3.34A over input Voltage Range

[7] Note: Testing was performed using a 3in. x 3in., four 2oz. copper layers, FR4 evaluation board platform.



PI3741-01-LGIZ Performance Characteristics  $T_A = 25^\circ\text{C}$

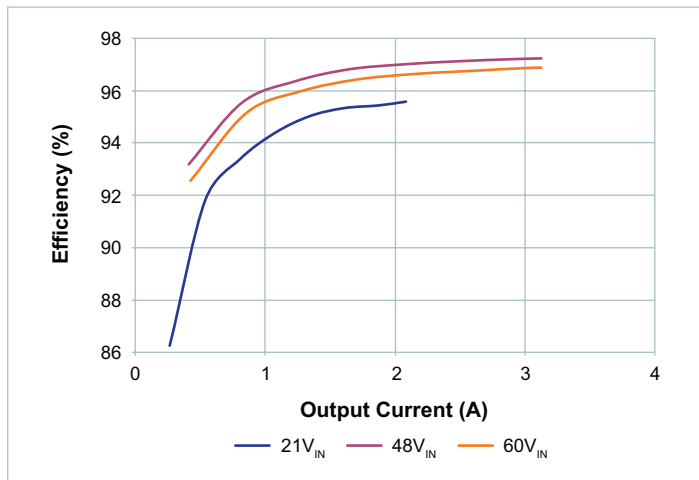


Figure 15 — 48V<sub>OUT</sub> Efficiency

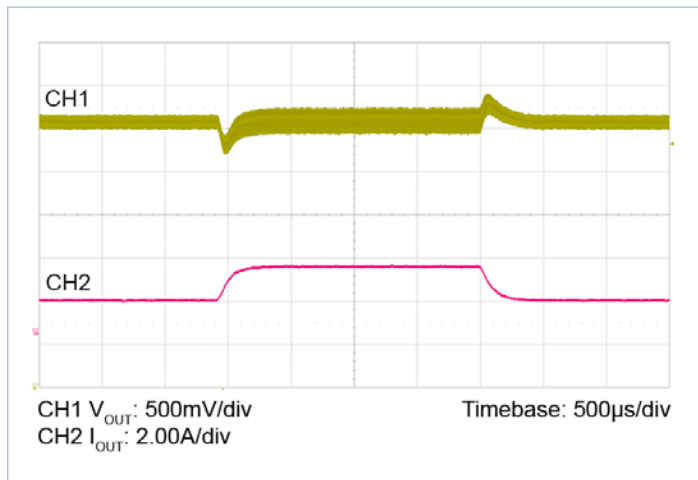


Figure 18 — 48V<sub>IN</sub> to 48V<sub>OUT</sub>, C<sub>OUT</sub> = 8 x 2.2µF Ceramic  
3.13A to 1.57A Load Step, 0.1A/µs

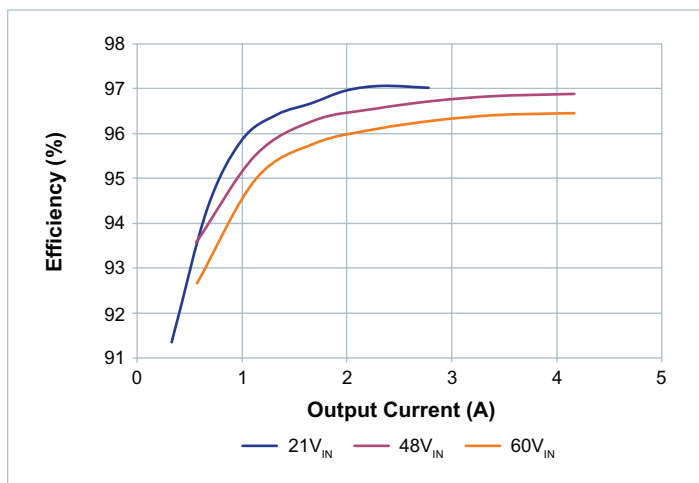


Figure 16 — 36V<sub>OUT</sub> Efficiency

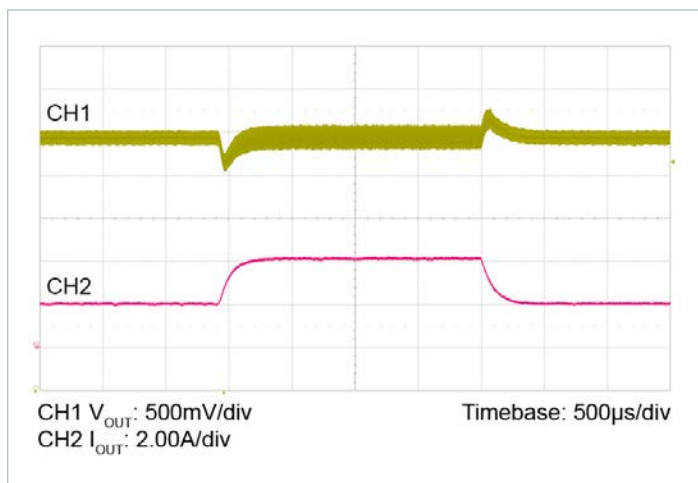


Figure 19 — 60V<sub>IN</sub> to 36V<sub>OUT</sub>, C<sub>OUT</sub> = 8 x 2.2µF Ceramic  
4.17A to 2.09A Load Step, 0.1A/µs

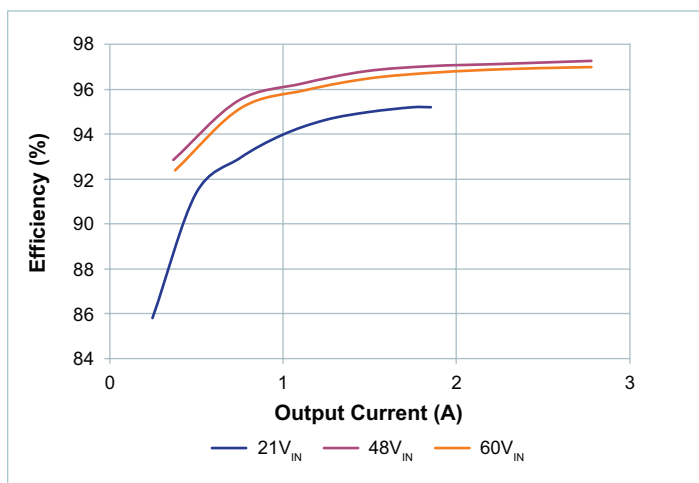


Figure 17 — 54V<sub>OUT</sub> Efficiency

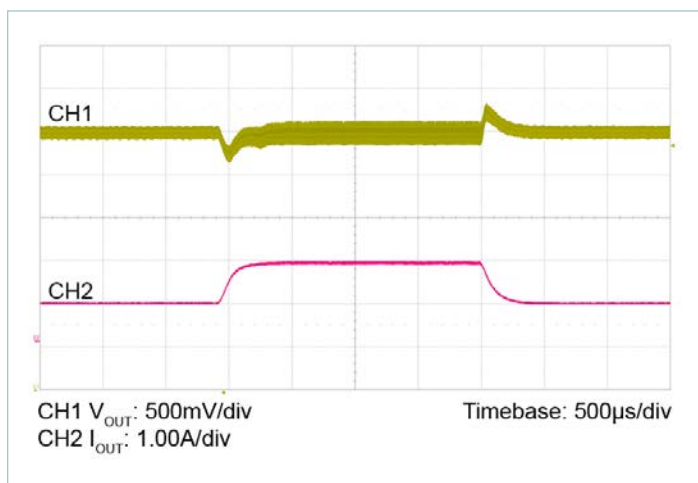


Figure 20 — 21V<sub>IN</sub> to 54V<sub>OUT</sub>, C<sub>OUT</sub> = 8 x 2.2µF Ceramic  
1.86A to 0.93A Load Step, 0.1A/µs

PI3741-01-LGIZ Performance Characteristics  $T_A = 25^\circ\text{C}$  (Cont.)

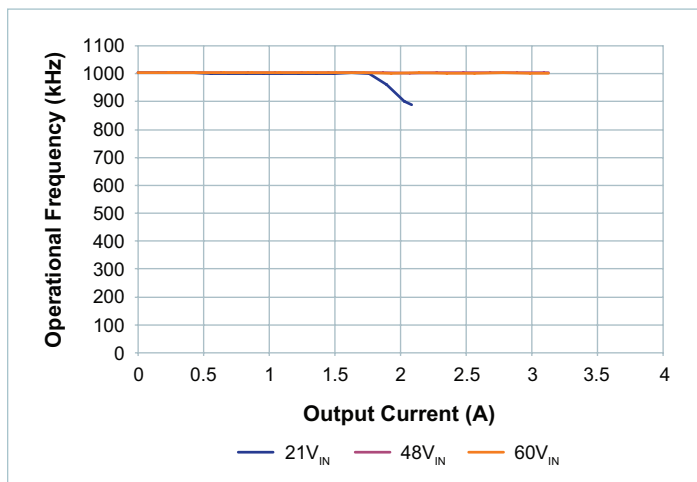


Figure 21 — Switching Frequency vs. Output Current @  $48V_{OUT}$

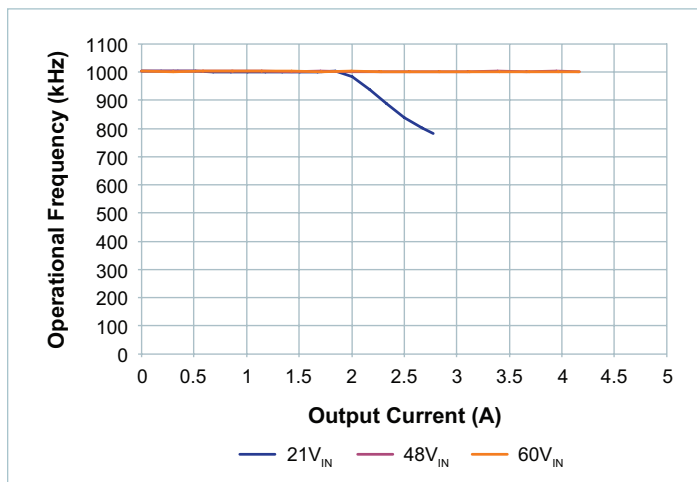


Figure 22 — Switching Frequency vs. Output Current @  $36V_{OUT}$

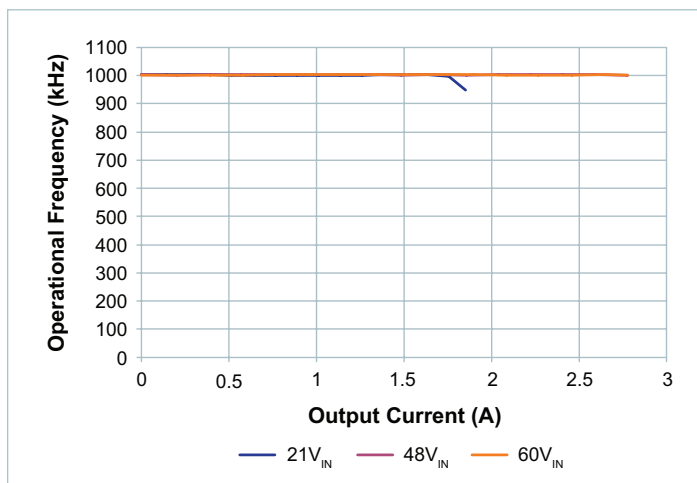


Figure 23 — Switching Frequency vs. Output Current @  $54V_{OUT}$

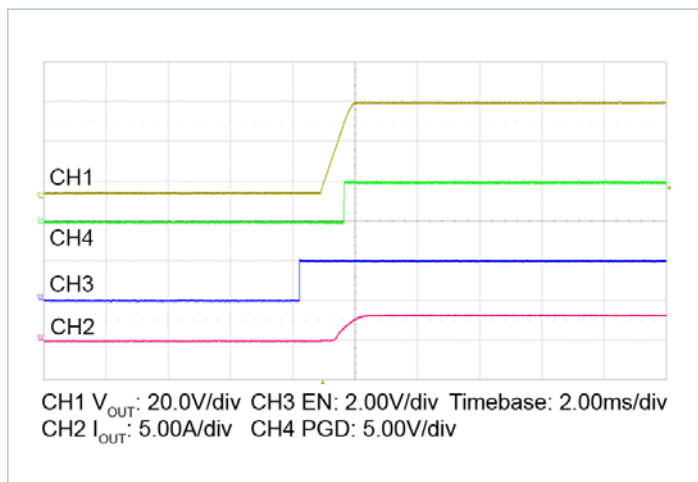


Figure 24 — Start-up with  $48V_{IN}$  to  $48V_{OUT}$  at 3.13A, Ext  $C_{SS} = 0\mu\text{F}$

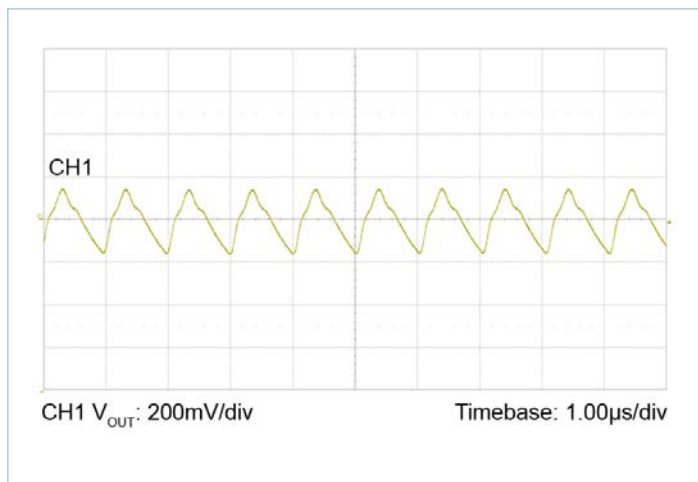


Figure 25 — Output voltage ripple at  $48V_{IN}$  to  $48V_{OUT}$ , 3.13A;  $C_{OUT} = 8 \times 2.2\mu\text{F}$  Ceramic

PI3741-01-LGIZ Efficiency & Power Loss  $T_A = 25^\circ\text{C}$  [7]

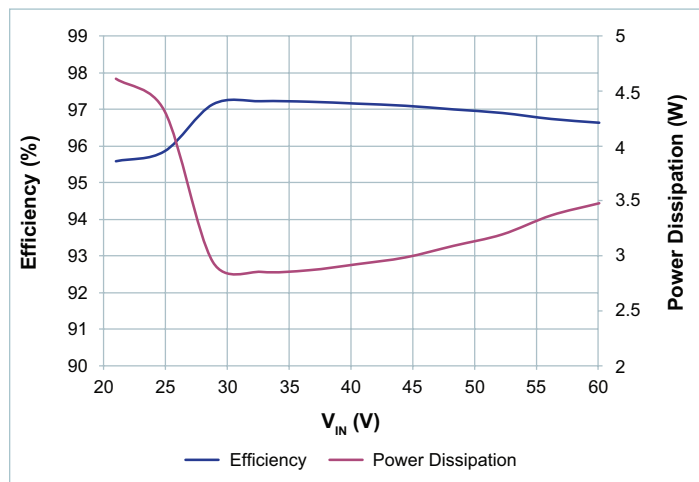


Figure 26 —  $48V_{OUT}$  Efficiency and Power Dissipation at 2.09A over input Voltage Range

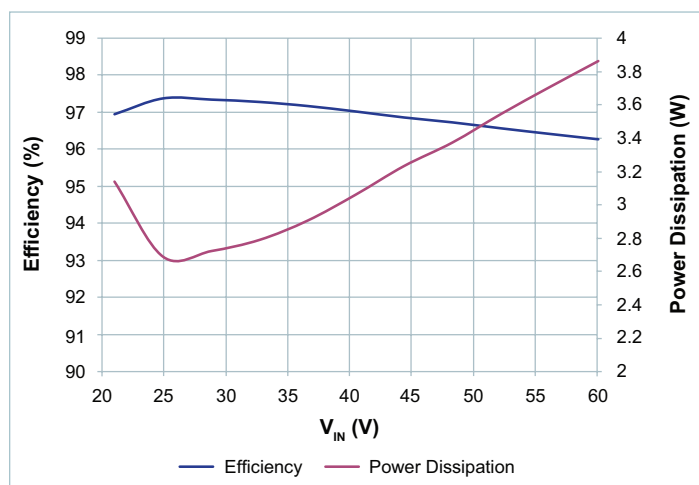


Figure 27 —  $36V_{OUT}$  Efficiency and Power Dissipation at 2.78A over input Voltage Range

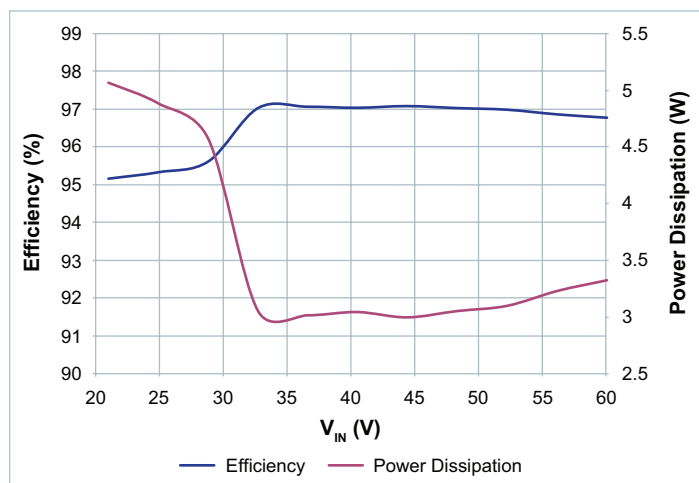


Figure 28 —  $54V_{OUT}$  Efficiency and Power Dissipation at 1.86A over input Voltage Range

[7] Note: Testing was performed using a 3in. x 3in., four 2oz. copper layers, FR4 evaluation board platform.

MTBF

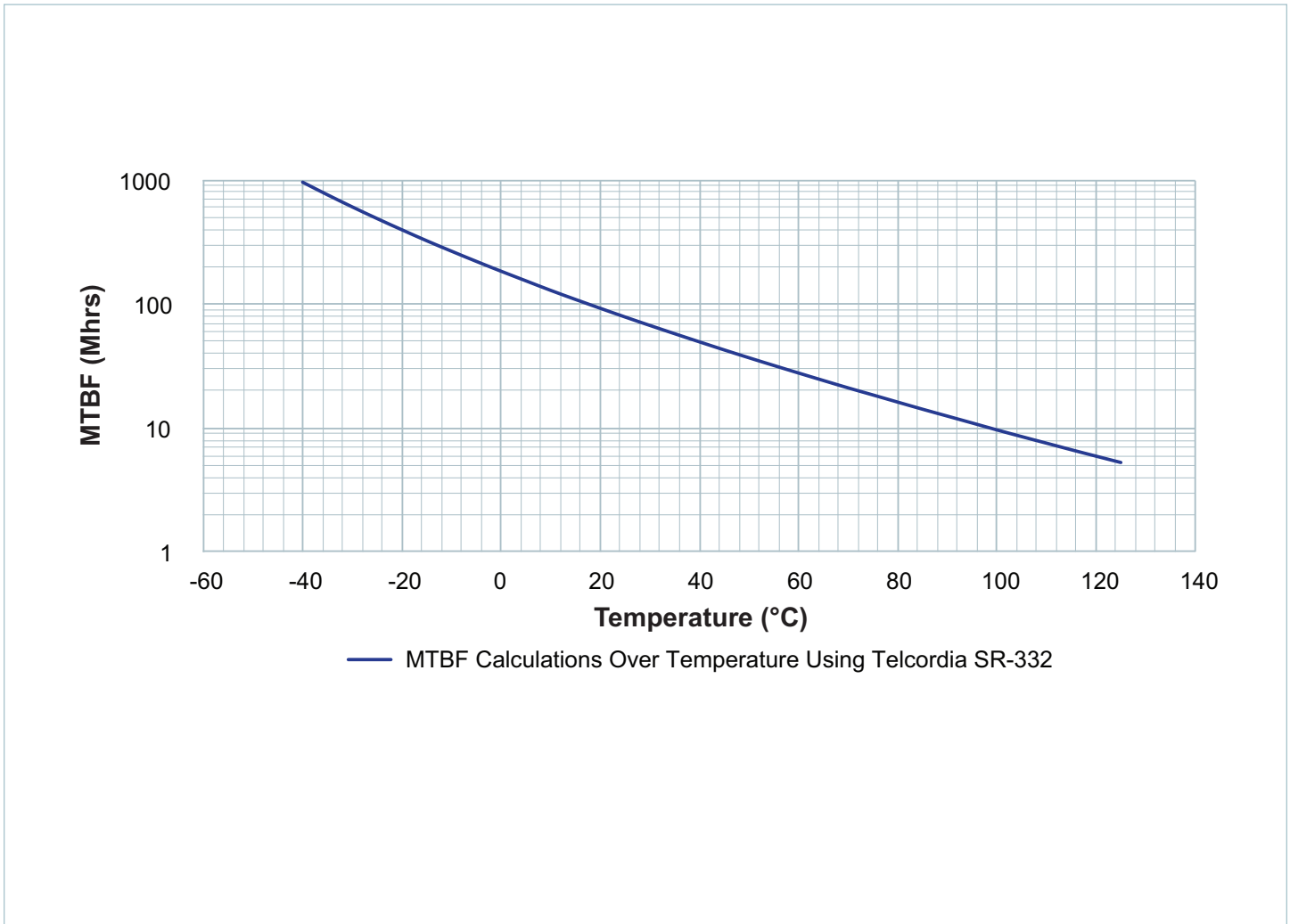


Figure 29 — PI3741-0x calculated MTBF Telcordia SR-332 GB

## Functional Description

The PI3741-0x is a family of highly integrated ZVS Buck-Boost regulators. The PI3741-0x has an adjustable output voltage that is set with a resistive divider. Performance and maximum output current are characterized with a specific external power inductor as defined in the electrical specifications, and in the inductor pairing section.

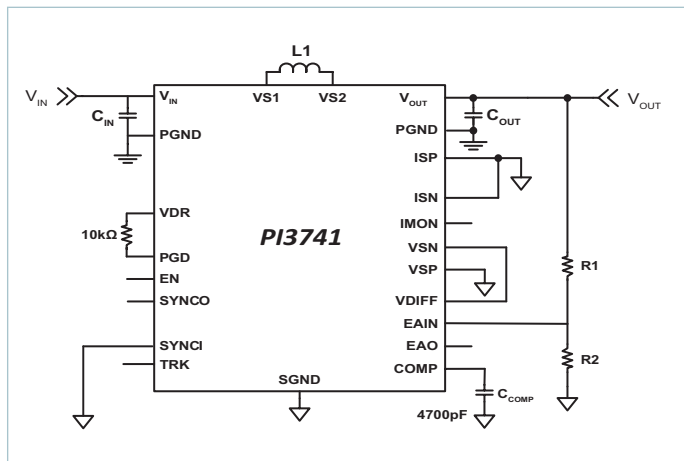


Figure 30 — ZVS Buck-Boost with required components

For basic operation, Figure 30 shows the minimum connections and components required.

### Enable

The EN pin of the regulator is referenced to SGND and permits the user to turn the regulator on or off. The EN polarity is a positive logic assertion. If the EN pin is left floating or asserted high, the regulator output is enabled. Pulling the EN pin below  $0.8V_{DC}$  with respect to SGND will discharge the SS/TRK pin until the output reaches zero or the EN pin is released. When the converter is disabled via the EN pin or due to a fault mode, the internal gate driver high side charge pumps are enabled as long as there is enough input voltage for the internal VDR supply voltage to be available. The return path for this charge pump supply is through the output. If the output load is disconnected or high impedance, the output capacitors will float up to about 3.4V maximum, sourced by  $960\mu A$  of leakage current. This pre-biased condition poses no issue for the converter. The  $960\mu A$  leakage current may be safely bypassed to SGND. A simple application circuit is available to bypass this current in a non-dissipative manner. Please contact Applications Engineering for details.

### Switching Frequency Synchronization

The SYNCI input allows the user to synchronize the controller switching frequency to the falling edge of an external clock referenced to SGND. The external clock can synchronize the unit between 50% and 110% of the preset switching frequency ( $F_{SW}$ ). The SYNCI pin should be connected to SGND when not in use, and should never be left floating.

### Soft-Start and Tracking

The PI3741-0x provides a soft start and tracking feature using the TRK pin. Programmable Soft Start requires an external capacitor from the TRK pin to SGND in addition to the internal

47nF soft-start capacitor to set the start-up ramp period greater than  $t_{SS}$ . The PI3741-0x internal reference and regulated output will proportionally follow the TRK ramp when it is below  $1.7V_{DC}$ . When the ramp is greater than  $1.7V_{DC}$ , the internal reference will remain at  $1.7V_{DC}$  while the TRK ramp rises and clamps at  $2.5V_{DC}$ . If the TRK pin goes below the disable threshold, the regulator will finish the current switching cycle and then stop switching.

### Remote Sensing Differential Amplifier

A general purpose operational amplifier is provided to assist with differential remote sensing and/or level shifting of the output voltage. The VDIFF pin can be connected to the transconductance error amplifier input EAIN pin, or with proper configuration can also be connected to the EAO pin to drive the modulator directly. If unused, connect in unity gain with VSP connected to SGND.

### Power Good

The PI3741-0x PGD pin functions as a power good indicator and pulls low when the regulator is not operating or if EAIN is less than 1.4V.

### Output Current Limit Protection

PI3741-0x has three methods implemented to protect from output short circuit or over current condition.

**Slow Current Limit protection:** prevents the regulator load from sourcing current higher than the maximum rated regulator current. If the output current exceeds the  $V_{OUT}$  Slow Current Limit ( $V_{OUT\_SCL}$ ) a slow current limit fault is initiated and the regulator is shutdown, which eliminates output current flow. After the Fault Restart Delay ( $t_{FR\_DLY}$ ), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

**Fast Current Limit protection:** monitors the external inductor current pulse-by-pulse to prevent the output from supplying saturation current. If the regulator senses a high inductor current pulse, it will initiate a fault and stop switching. After the Fault Restart Delay ( $t_{FR\_DLY}$ ), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

**Overload Timeout protection:** If the regulator is providing greater than the maximum output power for longer than the Overload Timeout delay ( $T_{OL}$ ), it will initiate a fault and stop switching. After Fault Restart Delay ( $t_{FR\_DLY}$ ), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the overload load is removed.

### Input Undervoltage Lockout

If  $V_{IN}$  falls below the input Undervoltage Lockout (UVLO) threshold, the PI3741-0x will complete the current cycle and stop switching. The system will restart once the input voltage is reestablished and after the Fault Restart Delay.

### Input Overvoltage Lockout

If  $V_{IN}$  rises above the input Overvoltage Lockout (OVLO) threshold, the PI3741-0x will complete the current cycle and stop switching. The system will restart once the input voltage is reestablished and after the Fault Restart Delay.

## Output Overvoltage Protection

The PI3741-0x family is equipped with two methods of detecting an output over voltage condition. To prevent damage to input voltage sensitive devices, if the output voltage exceeds 20% of its set regulated value as measured by the EAIN pin ( $V_{EAIN\_OV}$ ), the regulator will complete the current cycle, stop switching and issue an OVP fault. Also if the output voltage of the regulator exceeds the  $V_{OUT}$  Overvoltage Threshold ( $V_{OUT\_OVT}$ ) then the regulator will complete the current cycle, stop switching and issue an OVP fault. The system will resume operation once the output voltage falls below the OVP threshold and after Fault Restart Delay.

## Overtemperature Protection

The internal package temperature is monitored to prevent internal components from reaching their thermal maximum. If the Overtemperature Protection threshold is exceeded ( $T_{OTP}$ ), the regulator will complete the current switching cycle, enter a low power mode, set a fault flag, and will soft-start when the internal temperature decreases by more than the Overtemperature Restart Hysteresis ( $T_{OTP\_HYS}$ ).

## Pulse Skip Mode (PSM)

PI3741-0x features a hysteretic Pulse Skip Mode to achieve high efficiency at light loads. The regulator is setup to skip pulses if  $V_{EAO}$  falls below the Pulse Skip Threshold ( $V_{EAO\_PST}$ ). Depending on conditions and component values, this may result in single pulses or several consecutive pulses followed by skipped pulses. Skipping cycles significantly reduces gate drive power and improves light load efficiency. The regulator will leave Pulse Skip Mode once the control node rises above the Pulse Skip Mode threshold ( $V_{EAO\_PST}$ ).

## Variable Frequency Operation

The PI3741-0x is preprogrammed to a fixed, maximum, base operating frequency. The frequency is selected with respect to the required power stage inductor to operate at peak efficiency across line and load variations. The switching frequency period will stretch as needed during each cycle to accommodate low line and or high load conditions. By stretching the switching frequency period, thus decreasing the switching frequency, the ZVS operation is preserved throughout the input line voltage range maintaining optimum efficiency.

## IMON Amplifier

The PI3741-0x provides a differential amplifier with a level shifted, SGND referenced output, the IMON Pin, which is useful for sensing input or output current on high voltage rails. A fixed gain of 20:1 is provided over a large common mode range. When using the amplifier, the ISN pin must be referenced to the common mode voltage of the ISP pin for proper operation. See Absolute Maximum Ratings for more information. If not in use, the ISN and ISP pins should be connected to SGND and the IMON pin left floating.

## Application Description

### Output Voltage Trim

The output voltage can be adjusted by feeding back a portion of the desired output through a voltage divider to the error amplifier's input (see Figure 30). Equation 1 can be used to determine resistor values needed for the voltage divider.

$$R1 = R2 \cdot \left( \frac{V_{OUT}}{1.7} - 1 \right) \quad (1)$$

The R2 value is selected by the user; a 1.07kΩ resistor value is recommended.

If, for example, a 24V output is needed, the user can select a 1.07kΩ (1%) resistor for R2 and use Equation (1) to calculate R1. Once R1 value is calculated, the user should select the nearest resistor value available. In this example, R1 is 14.03kΩ so a 14.0kΩ should be selected.

### Soft-Start Adjustment and Tracking

The TRK pin offers a means to increase the regulator's soft-start time or to track with additional regulators. The soft-start slope is controlled by an internal 47nF and a fixed charge current to provide a minimum startup time of 1.6ms (typical). By adding an external capacitor to the TRK pin, the soft-start time can be increased further. The following equation can be used to calculate the proper capacitor for a desired soft-start times:

$$C_{TRK} = \frac{(t_{TRK} \cdot I_{SS})}{1.7} - 47 \cdot 10^{-9} \quad (2)$$

Where,  $t_{TRK}$  is the desired soft-start time and  $I_{SS}$  is the TRK pin source current (see Electrical Characteristics for limits).

The PI3741-0x allows the tracking of multiple like regulators. Two methods of tracking can be chosen: proportional or direct tracking. Proportional tracking will force all connected regulators to startup and reach regulation at the same time (see Figure 31 (a)). To implement proportional tracking, simply connect all devices TRK pins together.

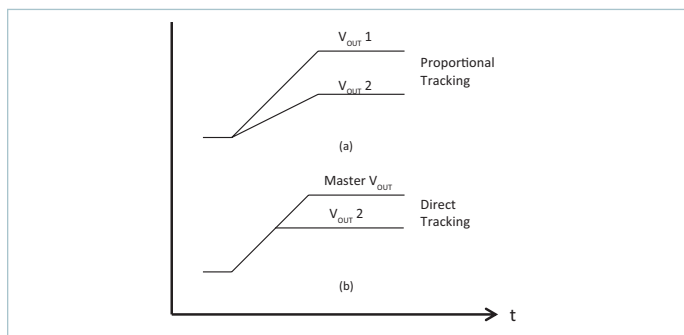


Figure 31 — PI3741-0x tracking methods

For Direct Tracking, choose the regulator with the highest output voltage as the master and connect the master to the TRK pin of the other regulators through a divider (Figure 32) with the same ratio as the slave's feedback divider (see Output Voltage Trim). The TRK pin should not be driven without 1k minimum series resistance.

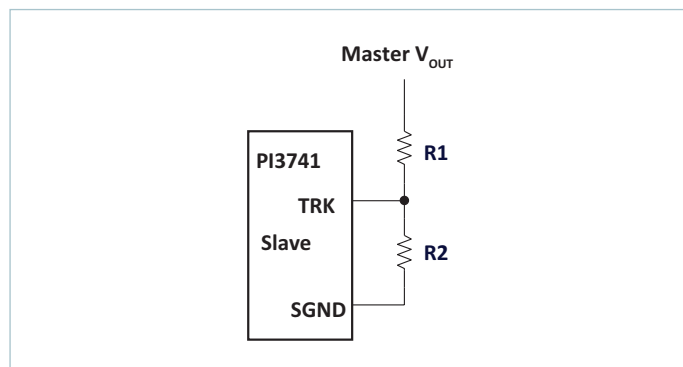


Figure 32 — Voltage divider connections for direct tracking

All connected regulators' soft-start slopes will track with this method. Direct tracking timing is demonstrated in Figure 31 (b). All tracking regulators should have their Enable (EN) pins connected together for proper operation.

### Inductor Pairing

Operations and characterization of the PI3741-0x was performed using a 900nH inductor, Part # HCV1206-R90-R, manufactured by Eaton. This Inductor has a form factor of 12.5mm x 10mm x 5mm. No other inductor is recommended for use with the PI3741-0x. For additional inductor information and sourcing, please contact Eaton directly.

**Filter Considerations**

The PI3741-0x requires low impedance ceramic input capacitors (X7R/X5R or equivalent) to ensure proper start up and high frequency decoupling for the power stage. The PI3741-0x will draw nearly all of the high frequency current from the low impedance ceramic capacitors when the main high side MOSFET(s) are conducting. During the time the MOSFET(s) are off, the input capacitors are replenished from the source. Table 1 shows the recommended input and output capacitors to be used for the PI3741-0x. Divide the total RMS current by the number of ceramic capacitors used to calculate the individual capacitor’s RMS current. Table 2 includes the recommended input and output ceramic capacitor. It is very important to verify that the voltage supply source as well as the interconnecting line are stable and do not oscillate.

**Input Filter case 1; Inductive source and local, external, input decoupling capacitance with negligible ESR (i.e.: ceramic type)**

The voltage source impedance can be modeled as a series  $R_{line}$   $L_{line}$  circuit. The high performance ceramic decoupling capacitors will not significantly damp the network because of their low ESR; therefore in order to guarantee stability the following conditions must be verified:

$$R_{line} > \frac{L_{line}}{(C_{IN\_INT} + C_{IN\_EXT}) \cdot |r_{EQ\_IN}|} \tag{3}$$

$$R_{line} \ll |r_{EQ\_IN}| \tag{4}$$

Where  $r_{EQ\_IN}$  can be calculated by dividing the lowest line voltage by the full load input current. It is critical that the line source impedance be at least an octave lower than the converter’s dynamic input resistance, Equation (4). However,  $R_{line}$  cannot be made arbitrarily low otherwise Equation (3) is violated and the system will show instability, due to under-damped RLC input network.

| $C_{INPUT}$<br>(see Table 2) | $C_{OUTPUT}$<br>(see Table 2) |
|------------------------------|-------------------------------|
| 5 X 2.2 $\mu$ F              | 8 X 2.2 $\mu$ F               |

**Table 1** — Recommended input and output capacitance

| Part Number       | Description                               | MFG Description |
|-------------------|---|-----------------|
| GRM32ER72A225KA35 | 2.2 $\mu$ F Capacitor, X7R 20% 100V, 1210 | Murata          |

**Table 2** — Capacitor manufacturer part numbers

**Input Filter case 2; Inductive source and local, external input decoupling capacitance with significant  $R_{C_{IN\_EXT}}$  ESR (i.e.: electrolytic type)**

In order to simplify the analysis in this case, the voltage source impedance can be modeled as a simple inductor  $L_{line}$ . Notice that the high performance ceramic capacitors  $C_{IN\_INT}$  within the PI3741-0x should be included in the external electrolytic capacitance value for this purpose. The stability criteria will be:

$$|r_{EQ\_IN}| > R_{C_{IN\_EXT}} \tag{5}$$

$$\frac{L_{line}}{C_{IN\_INT} \cdot R_{C_{IN\_EXT}}} < |r_{EQ\_IN}| \tag{6}$$

Equation (6) shows that if the aggregate ESR is too small – for example by using very high quality input capacitors ( $C_{IN\_EXT}$ ) – the system will be under-damped and may even become destabilized. Again, an octave of design margin in satisfying Equation (5) should be considered the minimum.

Note: When applying an electrolytic capacitor for input filter damping the ESR value must be chosen to avoid loss of converter efficiency and excessive power dissipation in the electrolytic capacitor.

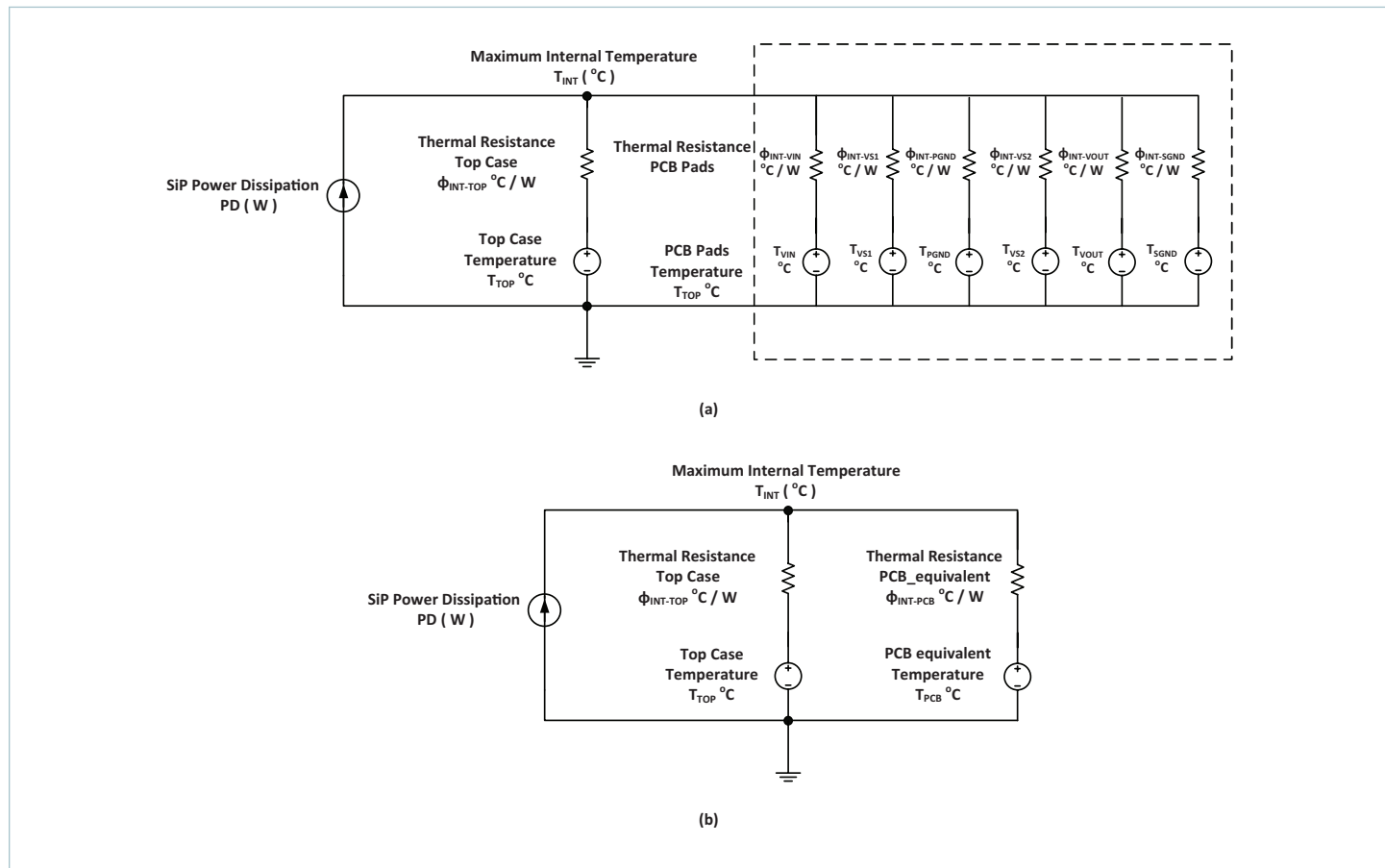


| Part Number    | V <sub>OUT</sub> (V) | V <sub>IN</sub> (V) | I <sub>OUT</sub> (A) | C <sub>INPUT</sub> Ripple Current (I <sub>RMS</sub> ) | C <sub>OUTPUT</sub> Ripple Current (I <sub>RMS</sub> ) | Output Ripple (mVpp) | Input Ripple (mVpp) |
|----------------|----------------------|---------------------|----------------------|---|--|----------------------|---------------------|
| PI3741-00-LGIZ | 21                   | 21                  | 4.29                 | 3.80  | 3.60   | 212                  | 298                 |
|                | 21                   | 48                  | 5.72                 | 3.91  | 4.41   | 202                  | 562                 |
|                | 21                   | 60                  | 5.72                 | 3.67  | 4.65   | 184                  | 558                 |
|                | 24                   | 21                  | 4.17                 | 4.31  | 4.19   | 238                  | 315                 |
|                | 24                   | 48                  | 5.42                 | 3.86  | 4.26   | 190                  | 512                 |
|                | 24                   | 60                  | 5.42                 | 3.68  | 4.55   | 193                  | 583                 |
|                | 28                   | 21                  | 3.58                 | 3.83  | 3.95   | 279                  | 340                 |
|                | 28                   | 48                  | 5.00                 | 3.76  | 4.06   | 210                  | 501                 |
|                | 28                   | 60                  | 5.00                 | 3.60  | 4.39   | 240                  | 621                 |
|                | 32                   | 21                  | 3.29                 | 4.36  | 4.39   | 308                  | 378                 |
|                | 32                   | 48                  | 4.38                 | 3.56  | 3.87   | 255                  | 509                 |
|                | 32                   | 60                  | 4.38                 | 3.50  | 4.28   | 264                  | 590                 |
|                | 36                   | 21                  | 3.34                 | 5.22  | 4.82   | 345                  | 423                 |
|                | 36                   | 48                  | 3.89                 | 3.46  | 3.76   | 280                  | 507                 |
|                | 36                   | 60                  | 3.89                 | 3.43  | 4.15   | 279                  | 588                 |
| PI3741-01-LGIZ | 36                   | 21                  | 2.78                 | 3.76  | 3.86   | 197                  | 263                 |
|                | 36                   | 48                  | 4.17                 | 4.46  | 4.90   | 293                  | 532                 |
|                | 36                   | 60                  | 4.17                 | 4.32  | 5.24   | 294                  | 602                 |
|                | 40                   | 21                  | 2.5                  | 4.05  | 3.98   | 215                  | 344                 |
|                | 40                   | 48                  | 3.75                 | 4.35  | 4.76   | 308                  | 534                 |
|                | 40                   | 60                  | 3.75                 | 4.25  | 5.10   | 302                  | 591                 |
|                | 48                   | 21                  | 2.09                 | 4.28  | 3.94   | 294                  | 334                 |
|                | 48                   | 48                  | 3.13                 | 4.18  | 4.43   | 319                  | 520                 |
|                | 48                   | 60                  | 3.13                 | 4.12  | 4.75   | 320                  | 576                 |
|                | 54                   | 21                  | 1.86                 | 4.50  | 3.92   | 289                  | 331                 |
|                | 54                   | 48                  | 2.78                 | 4.03  | 4.15   | 340                  | 528                 |
| 54             | 60                   | 2.78                | 4.00                 | 4.50  | 336  | 578                  |                     |

**Table 3** — Typical input and output ripple current/voltage with the recommended input and output capacitor recommended in Tables 1 and 2.

**Thermal Design**

Figure 33 (a) shows a thermal impedance model that can predict the maximum temperature of the highest temperature component for a given operating condition. This model assumes that all customer PCB connections are at one temperature, which is PCB equivalent Temperature  $T_{PCB}$  °C. The model can be simplified as shown in Figure 33 (b).



**Figure 33** — PI3741-0x SiP Thermal Model (a) and its simplified version (b).

Where the symbol in Figure 33 is defined as the following:

|                   |   |
|-------------------|---|
| $\phi_{INT-TOP}$  | is defined as the thermal impedance from the hottest component junction inside the SiP to the top side of the package.  |
| $\phi_{INT-PCB}$  | is defined as the thermal impedance from the hottest component junction inside the SiP to the circuit board it is mounted on, assuming all customer PCB connections at one temperature. |
| $\phi_{INT-VIN}$  | is defined as the thermal impedance from the hottest component junction inside the SiP to the circuit board it is mounted on at the $V_{IN}$ pad.                                       |
| $\phi_{INT-VS1}$  | is defined as the thermal impedance from the hottest component junction inside the SiP to the circuit board it is mounted on at the VS1 pad.  |
| $\phi_{INT-PGND}$ | is defined as the thermal impedance from the hottest component junction inside the SiP to the circuit board it is mounted on at the PGND pad.   |
| $\phi_{INT-VS2}$  | is defined as the thermal impedance from the hottest component junction inside the SiP to the circuit board it is mounted on at the VS2 pad.  |
| $\phi_{INT-VOUT}$ | is defined as the thermal impedance from the hottest component junction inside the SiP to the circuit board it is mounted on at the $V_{OUT}$ pad.                                      |
| $\phi_{INT-SGND}$ | is defined as the thermal impedance from the hottest component junction inside the SiP to the circuit board it is mounted on at the SGND pad.   |

The following equation can predict the junction temperature based on the heat load applied to the SiP and the known ambient conditions with the simplified thermal circuit model:

$$T_{INT} = \frac{PD + \frac{T_{TOP}}{\phi_{INT-TOP}} + \frac{T_{PCB}}{\phi_{INT-PCB}}}{\frac{1}{\phi_{INT-TOP}} + \frac{1}{\phi_{INT-PCB}}} \quad (7)$$

| Device         | Thermal Impedance            |                              |                              |                               |                              |                               |                               | Thermal Impedance with the simplified version |                              |
|----------------|------------------------------|------------------------------|------------------------------|-------------------------------|------------------------------|-------------------------------|-------------------------------|---|------------------------------|
|                | $\phi_{INT-TOP}$<br>(°C / W) | $\phi_{INT-VIN}$<br>(°C / W) | $\phi_{INT-VS1}$<br>(°C / W) | $\phi_{INT-PGND}$<br>(°C / W) | $\phi_{INT-VS2}$<br>(°C / W) | $\phi_{INT-VOUT}$<br>(°C / W) | $\phi_{INT-SGND}$<br>(°C / W) | $\phi_{INT-TOP}$<br>(°C / W)                  | $\phi_{INT-PCB}$<br>(°C / W) |
| PI3741-00-LGIZ | 42.48                        | 4.95                         | 24.95                        | 22.36                         | 44.26                        | 5.16                          | 177.10                        | 42.48   | 1.88                         |
| PI3741-01-LGIZ | 43.52                        | 5.14                         | 33.36                        | 22.30                         | 12.78                        | 7.25                          | 186.56                        | 43.52   | 1.95                         |

Table 4 — PI3741-0x SiP Thermal Impedance

Figure 34 shows a thermal impedance model that can predict the maximum hot spot temperature of the inductor for a given operating condition. This model assumes that all customer PCB connections are at one temperature, which is PCB equivalent Temperature  $T_{PCB}$  °C. If the inductor top and bottom are not mounted to a heat sink, the simplified model is parallel combination of all resistances that connect to the PCB.

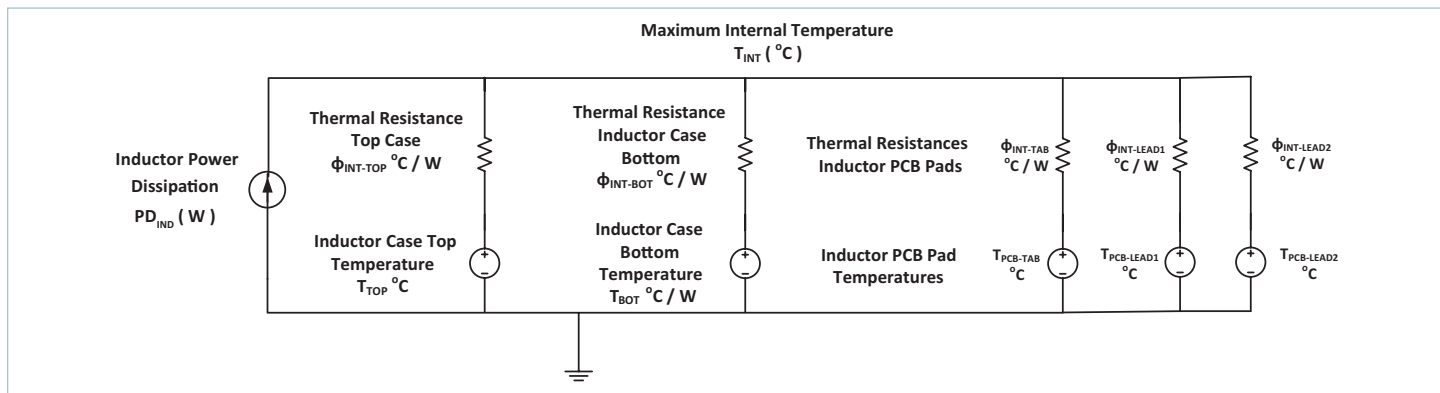


Figure 34 — PI3741-0x Inductor Thermal Impedance Model

Where the symbol in Figure 34 is defined as the following:

|                    |  |
|--------------------|--|
| $\phi_{INT-TOP}$   | is defined as the thermal impedance from the hot spot to the top surface of the core.  |
| $\phi_{INT-PCB}$   | is defined as the thermal impedance from the hot spot to the circuit board it is mounted on, assuming all customer PCB connections are at one temperature.                             |
| $\phi_{INT-BOT}$   | is defined as the thermal impedance from the hot spot to the bottom surface of the core.   |
| $\phi_{INT-TAB}$   | is defined as the thermal impedance from the hot spot to the metal mounting tab on the core body.  |
| $\phi_{INT-LEAD1}$ | is defined as the thermal impedance from the hot spot to one of the mounting leads. Since the leads are the same thermal impedance, there is no need to specify by explicit pin number |
| $\phi_{INT-LEAD2}$ | is defined as the thermal impedance from the hot spot to the other mounting lead   |

The following equation can predict the junction temperature based on the heat load applied to the inductor and the known ambient conditions with the simplified thermal circuit model:

$$T_{HOT SPOT} = \frac{PD + \frac{T_{TOP}}{\phi_{INT-TOP}} + \frac{T_{PCB}}{\phi_{INT-PCB}}}{\frac{1}{\phi_{INT-TOP}} + \frac{1}{\phi_{INT-PCB}}} \quad (8)$$

| Device   | Thermal Impedance         |                           |                           |                             |                             | Thermal Impedance with the simplified version |                           |
|----------|---------------------------|---------------------------|---------------------------|-----------------------------|-----------------------------|---|---------------------------|
|          | $\phi_{INT-TOP}$ (°C / W) | $\phi_{INT-BOT}$ (°C / W) | $\phi_{INT-TAB}$ (°C / W) | $\phi_{INT-LEAD1}$ (°C / W) | $\phi_{INT-LEAD2}$ (°C / W) | $\phi_{INT-TOP}$ (°C / W)                     | $\phi_{INT-PCB}$ (°C / W) |
| Inductor | 24.3                      | 9.67                      | 44.5                      | 34.0                        | 34.0                        | 24.3  | 12.24                     |

Table 5 — PI3741-0x Inductor Thermal Impedance

An estimation of SIP power loss to total loss percentage is shown in the following charts.

PI3741-00-LGIZ Percentage of SIP Loss to Total Loss

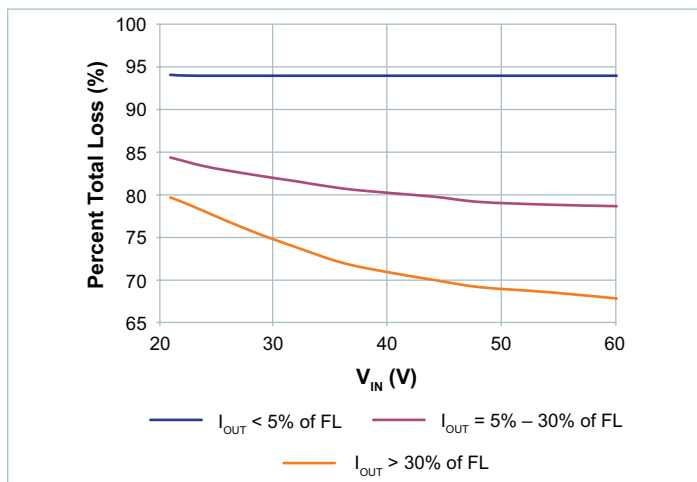


Figure 35 —  $V_{OUT} = 21V$

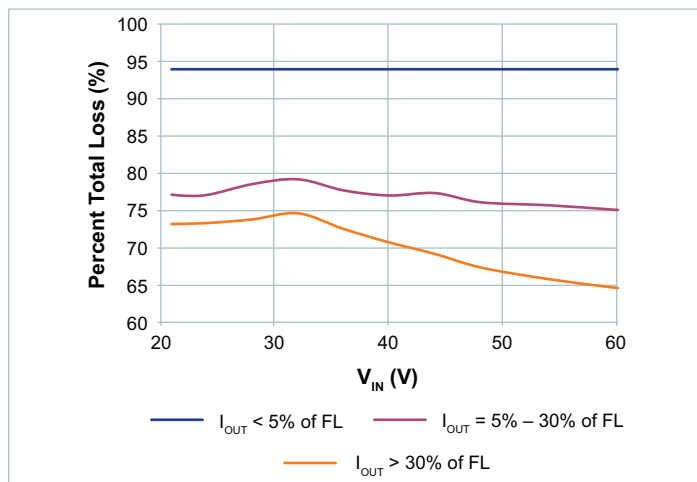


Figure 38 —  $V_{OUT} = 32V$

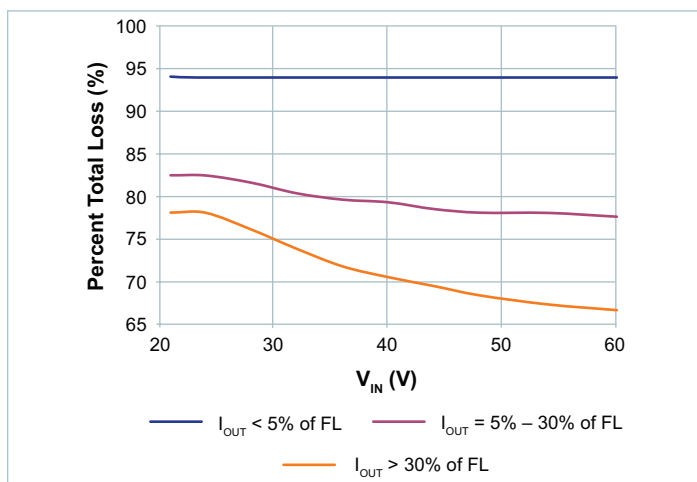


Figure 36 —  $V_{OUT} = 24V$

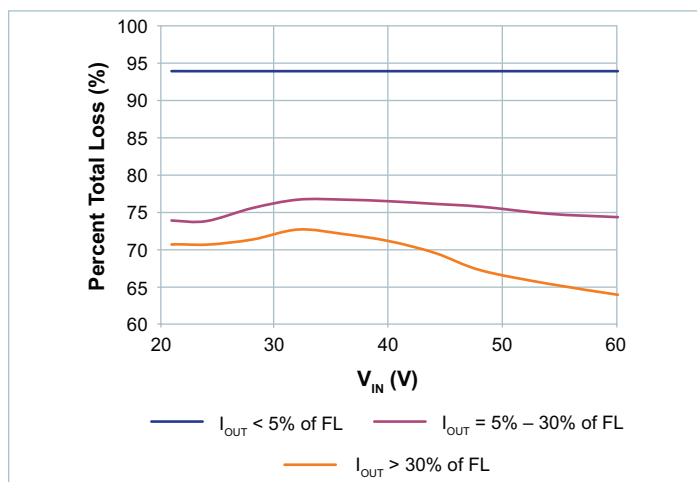


Figure 39 —  $V_{OUT} = 36V$

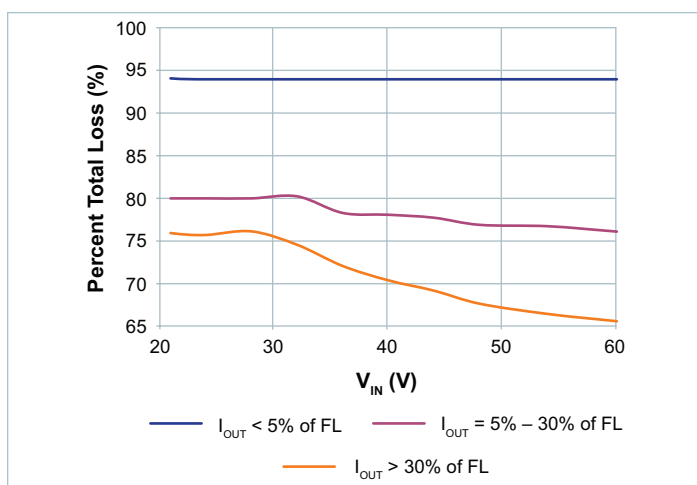


Figure 37 —  $V_{OUT} = 28V$

PI3741-01-LGIZ Percentage of SIP Loss to Total Loss

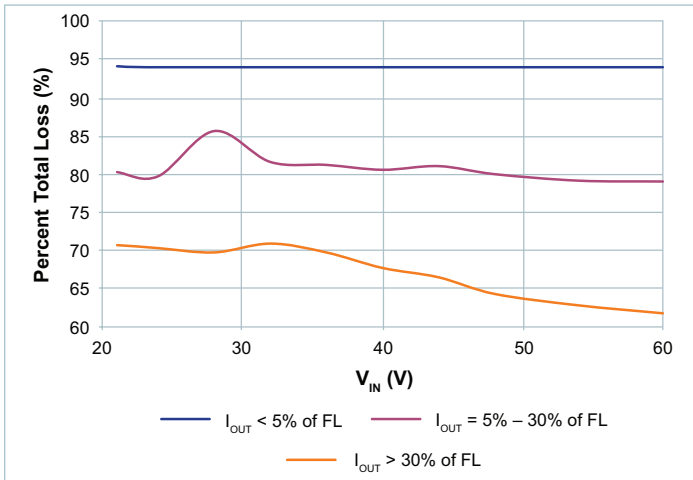


Figure 40 —  $V_{OUT} = 36V$

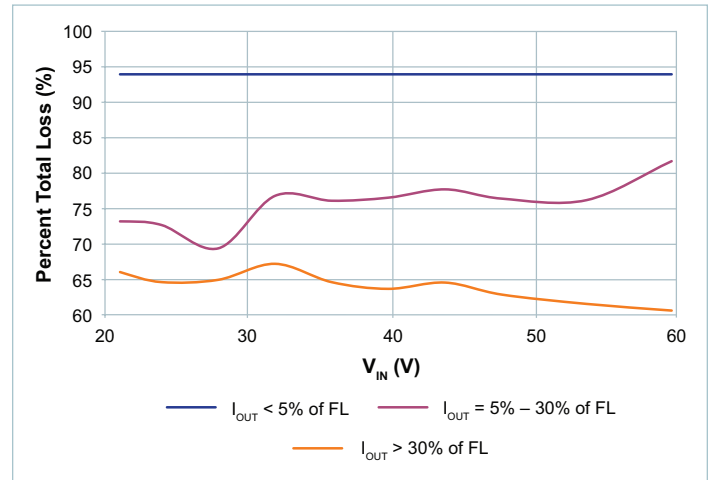


Figure 43 —  $V_{OUT} = 48V$

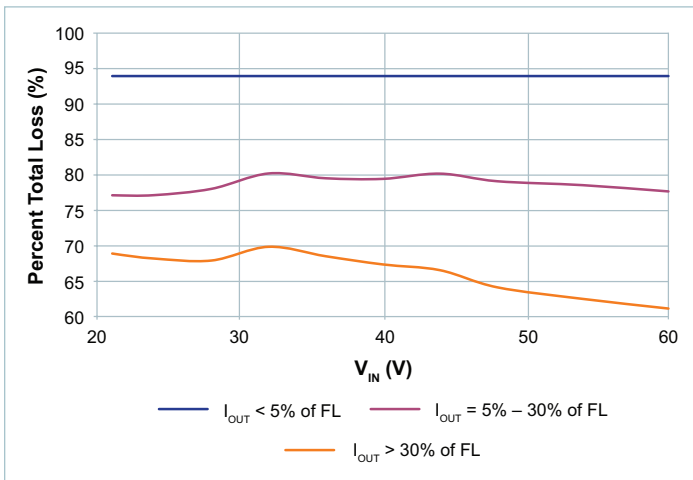


Figure 41 —  $V_{OUT} = 40V$

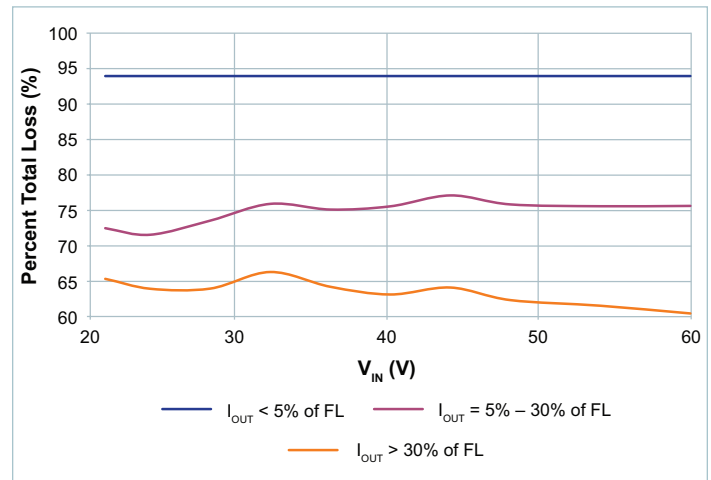


Figure 44 —  $V_{OUT} = 50V$

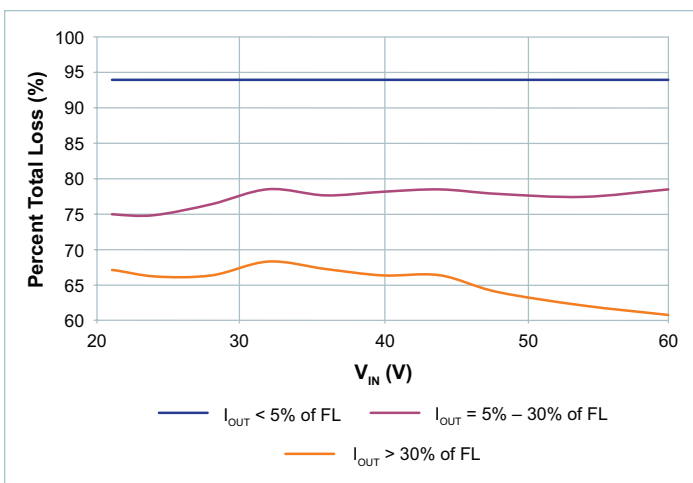


Figure 42 —  $V_{OUT} = 44V$

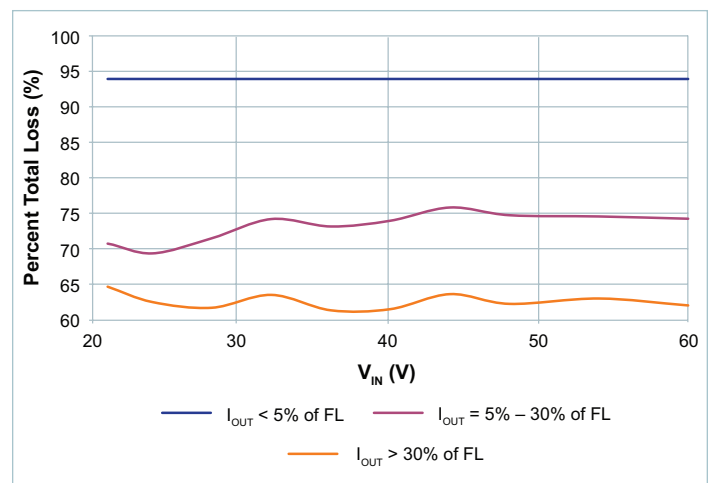


Figure 45 —  $V_{OUT} = 54V$

### Evaluation Board Thermal De-rating

Thermal de-rating curves are provided that are based on component temperature changes versus load current, input voltage and no air flow. It is recommended to use these curves as a guideline for proper thermal de-rating. These curves represent the entire system and are inclusive to both the Vicor SiP and the external inductor. Maximum thermal operation is limited by either the MOSFETs or inductor depending upon line and load conditions.

All thermal testing was performed using a 3in. x 3in., four 2oz. copper layers, FR4 evaluation board platform. Thermal measurements were made on the four internal MOSFETs and the external inductor.

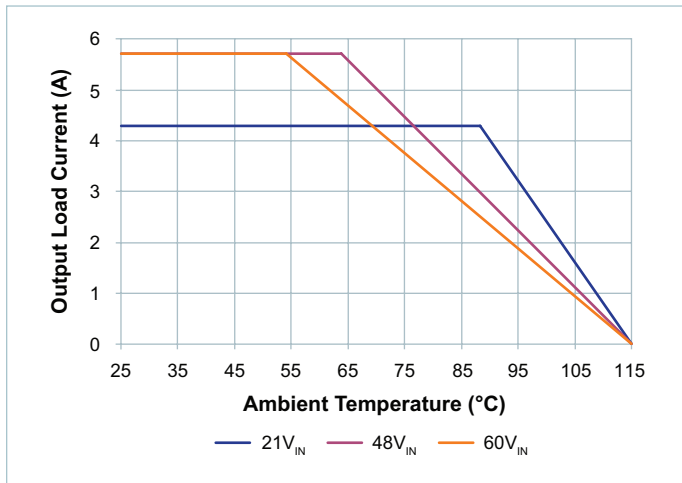


Figure 46 — Thermal de-rating for PI3741-00 evaluation board at V<sub>OUT</sub> = 21V, 0LFM

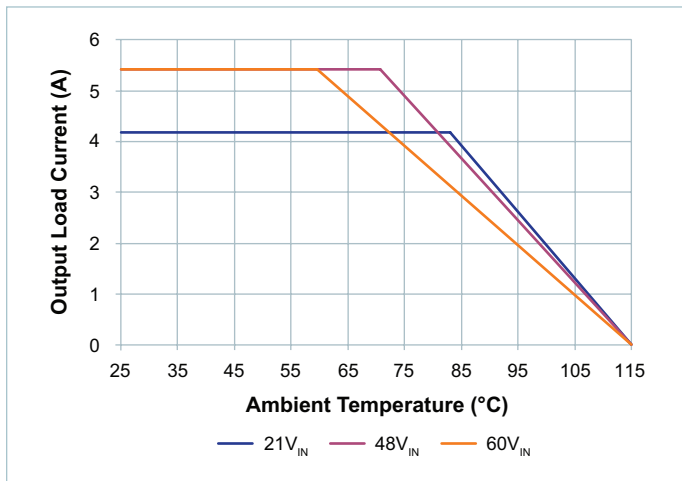


Figure 47 — Thermal de-rating PI3741-00 evaluation board at V<sub>OUT</sub> = 24V, 0LFM

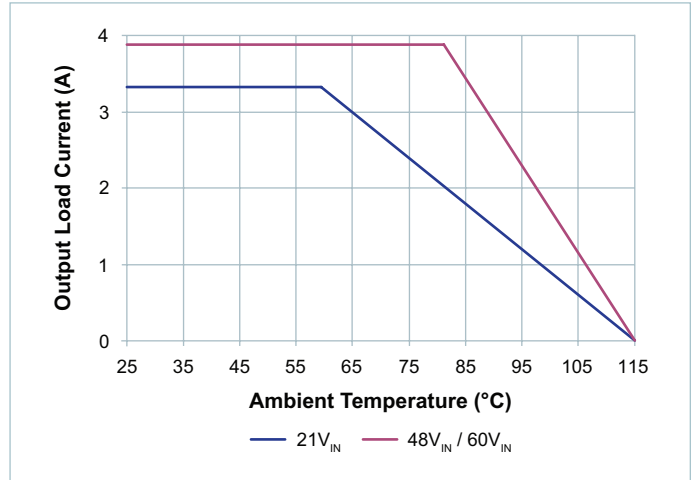


Figure 48 — Thermal de-rating for PI3741-00 evaluation board at V<sub>OUT</sub> = 36V, 0LFM

Evaluation Board Thermal De-rating (Cont.)

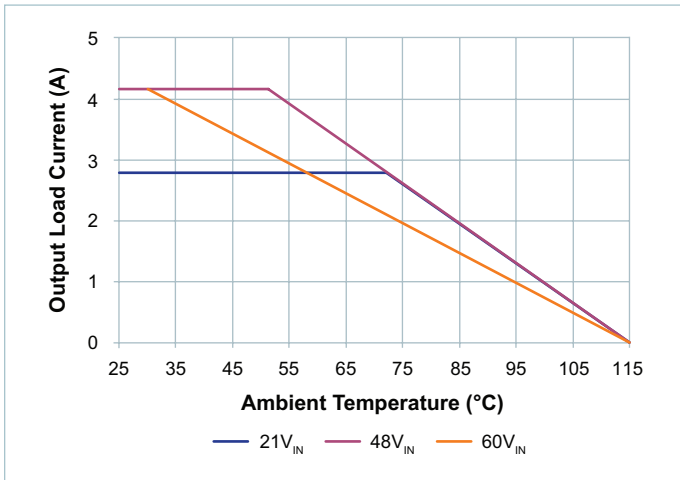


Figure 49 — Thermal de-rating for PI3741-01 evaluation board at  $V_{OUT} = 36V, 0LFM$

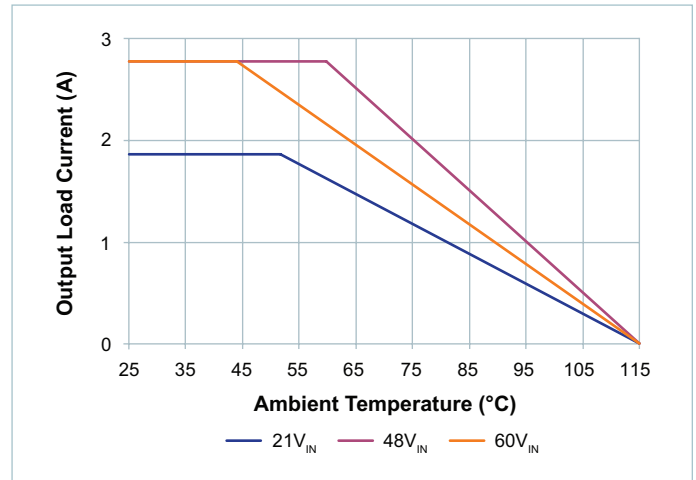


Figure 51 — Thermal de-rating for PI3741-01 evaluation board at  $V_{OUT} = 54V, 0LFM$

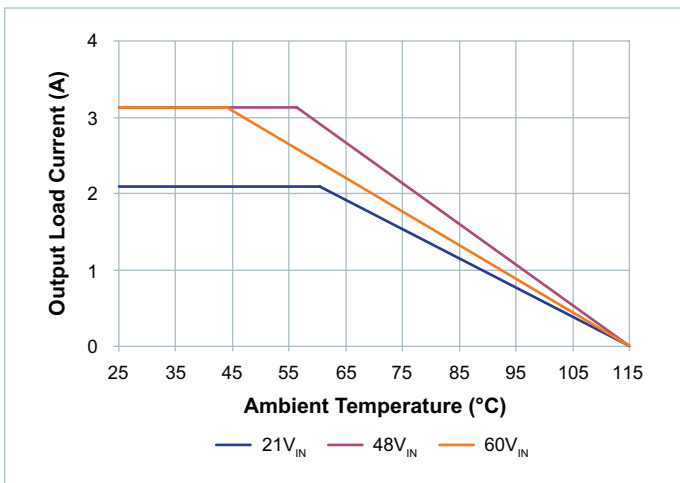


Figure 50 — Thermal de-rating PI3741-01 evaluation board at  $V_{OUT} = 48V, 0LFM$



## Parallel Operation

PI3741-0x can be connected in parallel to increase the output capability of a single output rail. When connecting modules in parallel, each EAO, TRK, EAIN and EN pin should be connected together. Current sharing will occur automatically in this manner so long as each inductor is the same value. A common viewing chain may be used to sense the output voltage. Up to three modules may be connected in parallel. The modules current sharing accuracy is determined by the inductor tolerance ( $\pm 10\%$ ) and to a lesser extent, timing variation ( $\pm 1.5\%$ ). Current sharing may be considered independent of synchronization and/or interleaving. Modules do not have to be interleaved or synchronized to share current. The following equation determines the output capability of N modules (up to three) to be determined:

$$I_{array} = I_{mod} + (I_{mod} \cdot (N - 1) \cdot 0.77) \quad (9)$$

Where:

$I_{array}$  is the maximum output current of the array

$I_{mod}$  is the maximum output per module

N is the number of modules

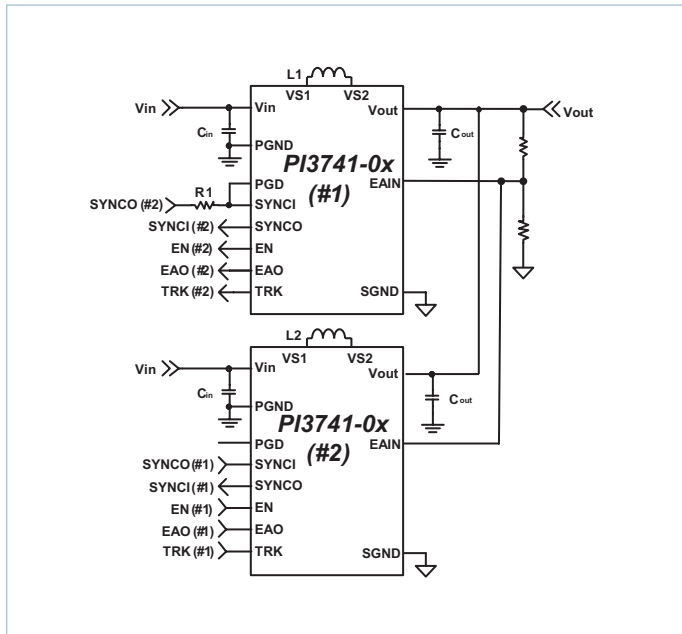


Figure 52 — PI3741-0x parallel operation

## Synchronization

PI3741-0x units may be synchronized to an external clock by driving the SYNCI pin. The synchronization frequency must not be higher than the programmed maximum value  $F_{SW}$ . This is the switching frequency during DCM of operation. The minimum synchronization frequency is  $F_{SW} / 2$ . In order to ensure proper power delivery during synchronization, the user should refer to the switching frequency vs. output current curves for the load current, output voltage and input voltage operating point. The synchronization frequency should not be lower than that determined by the curve or reduced output power will result. The power reduction is approximately the ratio between required frequency and synchronizing frequency. If the required frequency is 1MHz and the sync frequency is 600kHz, the user should expect a 40% reduction in output capability.

## Interleaving

Interleaving is primarily done to reduce output ripple and the required number of output capacitors by introducing phase current cancellation. The PI3741-0x has a fixed delay that is proportional to the maximum value of  $F_{SW}$  shown in the data sheet. When connecting two units as shown in Figure 52, they will operate at 180 degrees out of phase when the converters switching frequency is equal to  $F_{SW}$ . If the converter enters CrCM and the switching frequency is lower than  $F_{SW}$ , the phase delay will no longer be 180 degrees and ripple cancellation will begin to decay. Interleaving when the switching frequency is reduced to lower than 80% of the programmed maximum value is not recommended.

## VDR Bias Regulator

The VDR internal bias regulator is a ZVS switching regulator that resides internal to the PI3741-0x. It is intended strictly for use to power the internal controller and driver circuitry. The power capability of this regulator is sized only for the PI3741-0x, with adequate reserve for the application it was intended for. It may be used for as a pull-up source for open collector applications and for other very low power use with the following restrictions:

- No direct connection is allowed. Any noise source that can disturb the VDR voltage can also affect the internal controller operation.
- All loads must be locally de-coupled using a 0.1 $\mu$ F ceramic capacitor. This capacitor must be connected to the VDR output through a series resistor no smaller than 1k $\Omega$  which forms a loss pass filter and limits the total current to 5mA.

## System Design Considerations

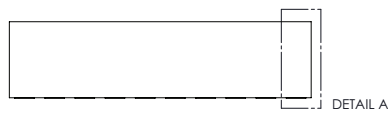
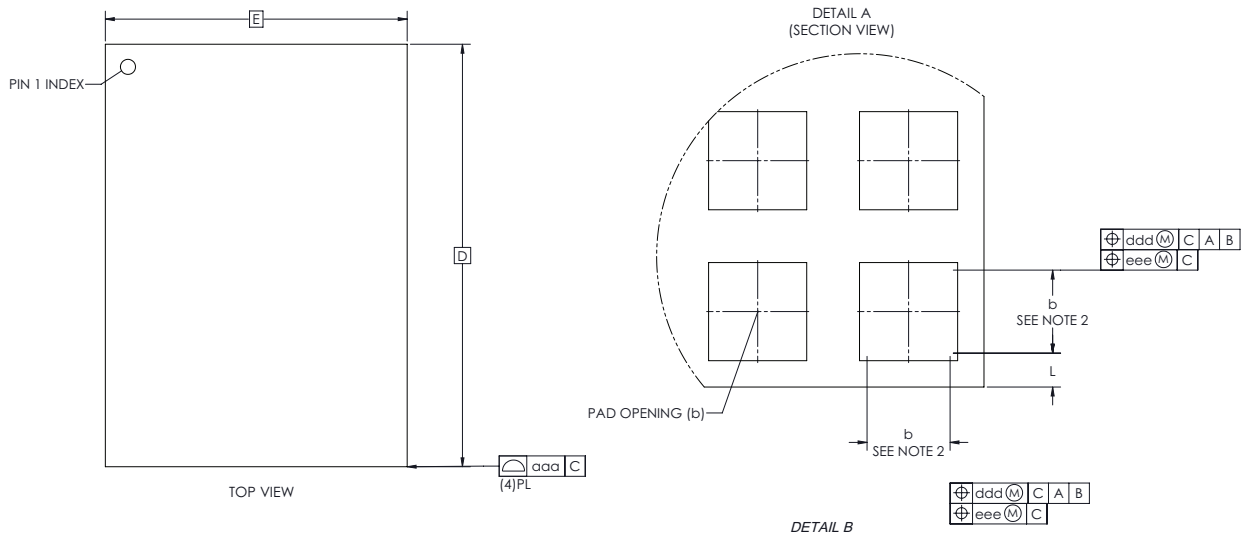
### Inductive Loads

As with all power electronic applications, consideration must be given to driving inductive loads that may be exposed to a fault in the system which could result in consequences beyond the scope of the power supply primary protection mechanisms. An inductive load could be a filter, fan motor or even excessively long cables. Consider an instantaneous short circuit through an un-damped inductance that occurs when the output capacitors are already at an initial condition of fully charged. The only thing that limits the current is the inductance of the short circuit and any series resistance. Even if the power supply is off at the time of the short circuit, the current could ramp up in the external inductor and store considerable energy. The release of this energy will result in considerable ringing, with the possibility of ringing nodes connected to the output voltage below ground. The system designer should plan for this by considering the use of other external circuit protection such as load switches, fuses, and transient voltage protectors. The inductive filters should be critically damped to avoid excessive ringing or damaging voltages. Adding a high current Schottky diode from the output voltage to PGND close to the PI741-0x is recommended for these applications.

### Low Voltage Operation

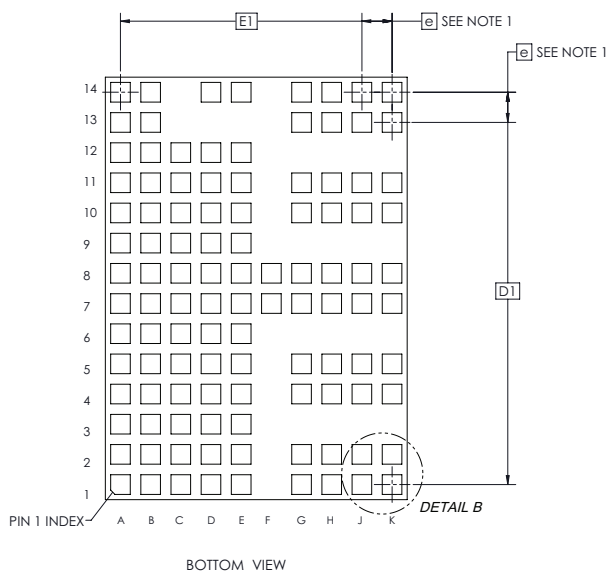
There is no isolation from an SELV (Safety-Extra-Low-Voltage) power system. Powering low voltage loads from input voltages as high as 60V may require additional consideration to protect low voltage circuits from excessive voltage in the event of a short circuit from input to output. A fast TVS (transient voltage suppressor) gating an external load switch is an example of such protection.

Package Drawings

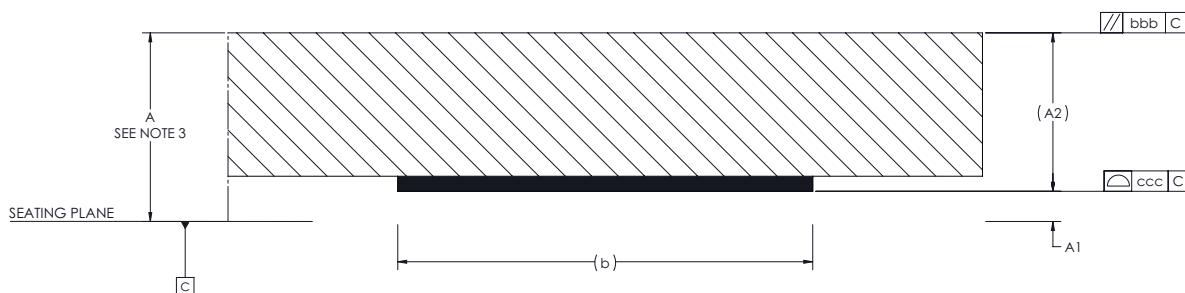


| BB 10x14mm SIP         |           |       |      |
|------------------------|-----------|-------|------|
| DIMENSIONAL REFERENCES |           |       |      |
| REF.                   | MIN.      | NOM.  | MAX. |
| A                      | 2.47      | 2.56  | 2.63 |
| A1                     | --        | --    | 0.04 |
| A2                     | --        | --    | 2.57 |
| b                      | 0.50      | 0.55  | 0.60 |
| D                      | 14.00 BSC |       |      |
| E                      | 10.00 BSC |       |      |
| D1                     | 13.00 BSC |       |      |
| E1                     | 9.00 BSC  |       |      |
| e                      | 1.00 BSC  |       |      |
| L                      | .175      | 0.225 | .275 |

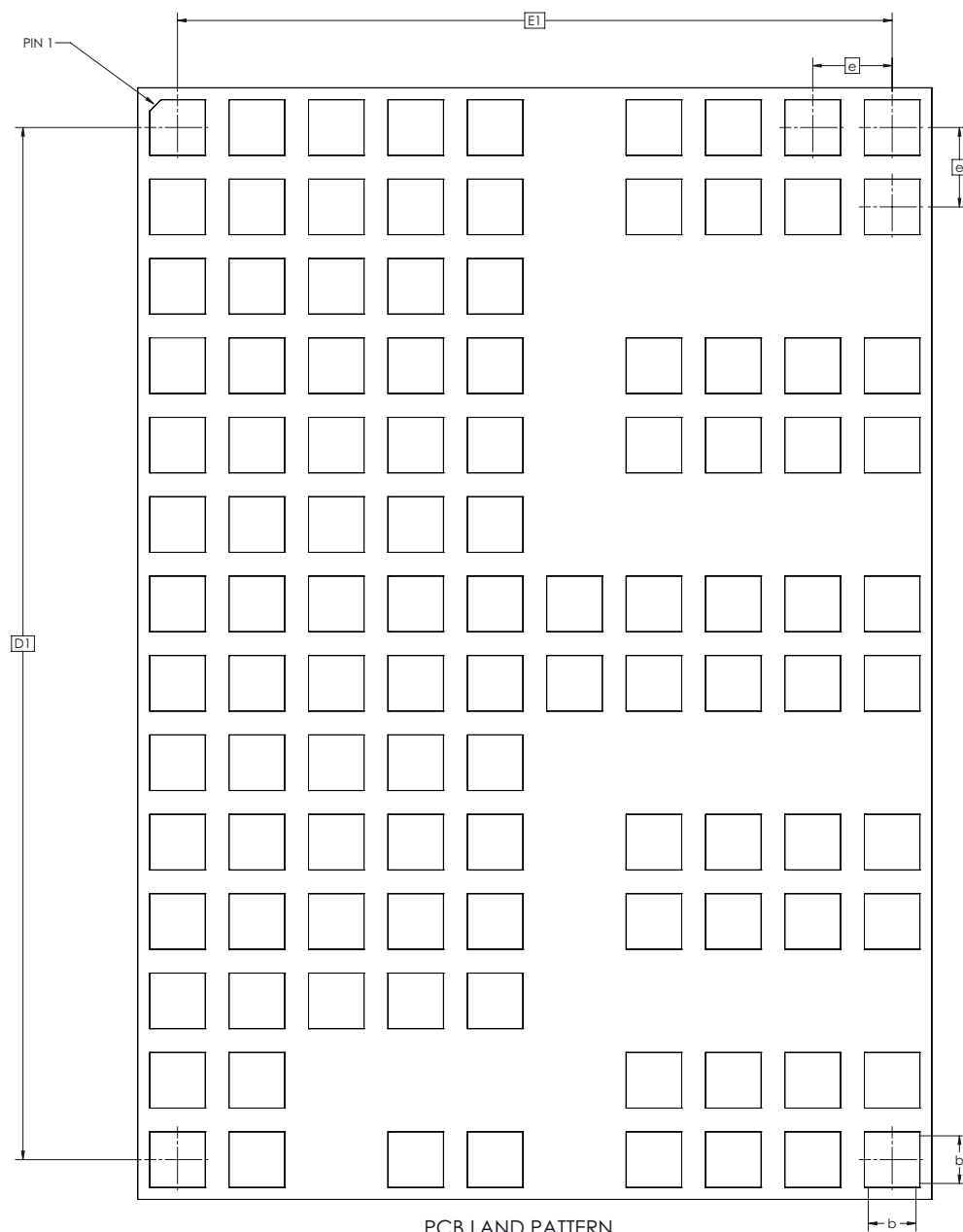
| BB 10x14mm SIP         |                                |
|------------------------|--------------------------------|
| DIMENSIONAL REFERENCES |                                |
| REF.                   | TOLERANCE OF FORM AND POSITION |
| aaa                    | 0.10                           |
| bbb                    | 0.10                           |
| ccc                    | 0.08                           |
| ddd                    | 0.10                           |
| eee                    | 0.08                           |



- NOTES:
1. 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.
  2. DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.00mm AND 0.25mm FROM TERMINAL TIP.
  3. DIMENSION 'A' INCLUDES PACKAGE WARPAGE
  4. EXPOSED METALLIZED PADS ARE Cu PADS WITH SURFACE FINISH PROTECTION.
  5. RoHS COMPLIANT PER CST-0001 LATEST REVISION.
  6. ALL DIMENSIONS ARE IN MM UNLESS OTHERWISE SPECIFIED.



Receiving PCB Pattern Design Recommendations



PCB LAND PATTERN  
BB 10x14mm SiP

| DIMENSIONAL REFERENCES |           |      |      |
|------------------------|-----------|------|------|
| REF.                   | MIN.      | NOM. | MAX. |
| b                      | 0.50      | 0.55 | 0.60 |
| D1                     | 13.00 BSC |      |      |
| E1                     | 9.00 BSC  |      |      |
| e                      | 1.00 BSC  |      |      |

Recommended receiving footprint for PI3741-0x 10mm x 14mm package. All pads should have a final copper size of 0.55mm x 0.55mm, whether they are solder-mask defined or copper defined, on a 1mm x 1mm grid. All stencil openings are 0.45mm when using either a 5mil or 6mil stencil.

## Revision History

| Revision | Date     | Description  | Page Number(s)     |
|----------|----------|--|--------------------|
| 1.0      | 08/29/16 | Initial Release  | n/a                |
| 1.1      | 08/31/16 | Update package drawings  | 6, 35, 36          |
| 1.2      | 02/08/17 | Corrections to Typical Application, Figure 30<br>Update package outline drawings | 1, 21<br>6, 35, 36 |
| 1.3      | 03/10/17 | Miscellaneous typo corrections   | 2, 8, 11           |
| 1.4      | 03/31/17 | Correct LGH pin name<br>Include additional PCB Pattern information               | 6<br>36            |

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